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Directorate of Distance Education

M.Sc. [Physics]

I - Semester

345 14

LABORATORY - I:

ADVANCED ELECTRONICS AND PHYSICS

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LABORATORY - I: ADVANCED ELECTRONICS AND PHYSICS

Syllabi

(Any Fifteen of the following)

1. Study the characteristics of FET.
2. Study the characteristics of transistor (CE mode).
3. Study the characteristics of Zener diode and construct regulated DC power supply.
4. Construct the logic gates using discrete components.
5. Design of FET amplifier - CS Configuration.
6. Characteristics of UJT.
7. Relaxation oscillator (UJT).
8. Transistor Astable multivibrator.
9. Monostable multivibrator (Transistor).
10. Transistorized Hartely and Colpitt's audio oscillator.
11. Calibration of Spectrograph – Iron or Copper spectrum.
12. Michelson's Interferometer.
13. q, n, - Elliptical fringes.
14. q, n, - Hyperbolic fringes.
15. Ultrasonic Interferometer – Construction of oscillator and measurements.
16. Babinet's Compensator and study of polarized light.
17. G.M Counter – Statistical probability, Absorption measurements, Half life.
18. Any of the experiments of equal standard.

INTRODUCTION

NOTES

Electronics is the application of electromagnetic and quantum theory of physics to construct devices that can perform useful tasks, from as simple as electrical heaters or light bulbs to as complex as the Large Hadron Collider. Electronics and electronic appliances have become essential for our life style in this era. With the advancement of science and technology, electronics has been introduced into industry in a large scale to meet the challenges of the growing requirement of the day. Starting from the fabrication of vacuum tubes to transistors, the science of electronics has moved rapidly to fabricate integrated circuits which in turn have paved the way for generating microprocessors, super computers and the advanced electronics gadgets of the day.

Now-a-days most of the electronic devices use semiconductor components to perform electron control. The study of semiconductor devices and related technology is considered a branch of solid-state physics, whereas the design and construction of electronic circuits to solve practical problems come under electronics engineering. Principally, the field of electronics comprises of the physics, engineering, technology and applications that deal with the emission, flow and control of electrons in vacuum and matter. The identification of the electron in 1897, along with the invention of the vacuum tube, which could amplify and rectify small electrical signals, inaugurated the field of electronics and the electron age.

An electronic component is any physical entity in an electronic system used to affect the electrons or their associated fields in a manner consistent with the intended function of the electronic system. Circuits and components can be divided into two groups: Analog and Digital. Analog circuits use a continuous range of voltage or current as opposed to discrete levels as in digital circuits. Examples of analog circuits include vacuum tube and transistor amplifiers, operational amplifiers and oscillators. Digital circuits are electric circuits based on a number of discrete voltage levels and use the most common physical representation of Boolean algebra forming the basis of all digital processors. A particular device may consist of circuitry that has one or the other or a mix of the two types.

Due to the complex nature of electronics theory, laboratory experimentation is considered as the significant measure for the development of electronic devices. These experiments are specifically used for testing or verifying the engineer's design and detecting errors.

This book, *Advanced Electronics and Physics*, focuses on the engineering aspects of electronics and provides the basic knowledge on transistor, diode, amplifier, oscillators, semiconductor, spectrometer, microscopes, multivibrator and Michelson's Interferometer.

NOTES

1. STUDY THE CHARACTERISTICS OF FET (FIELD EFFECT TRANSISTOR)

Introduction

A field effect transistor is a three terminal semiconductor device. These terminals are named as (a) Source, (b) Drain and (c) Gate. The path of current is from source to drain while the third terminal gate controls the flow of current in this path.

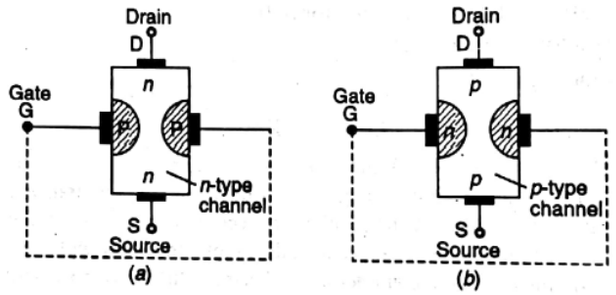

Fig. 1: *The Diagrams of Different Types of Field Effect Transistors*

The central channels can be a 'p' or an 'n-type' silicon bars having the junctions of opposite polarity on the sides. A diagram of FET having "n-type" channels is shown in Figure 1(a) and the one having a 'p-type' channel is shown in the next Figure 1(b).

The two part junctions of common gate terminal are internally conned which is shown in this figure by dotted lines. The Drain and Source terminals are taken out from the ends. The Drain and Source terminals are equivalent to each other and can be appointed as the drain or the source on the basis of choice (inter-changeable).

Working: We have a FET of n-channel type. A voltage V_{GS} can be applied between the Gate and the source terminals. Similarly, a voltage V_{DS} can be applied between the Source and the Drain as shown in the given arrangement (Refer Figure 2). Let us consider the gate voltage is zero in the beginning. When a voltage V_{DS} (Between Source and Drain) is applied. It is shown in the figure that the negative terminal of the battery providing V_{DS} is connected to the source and the positive terminal is connected to the Drain terminal D. Electrons flow from the Source to the Drain which gives the respective meaning to their names.

The two p-n junctions at the side of the bar establish a depletion layers and these electrons flow through a narrow channel between these depletion layers. The width of this channel between the depletion layers controls the flow of the number electrons and hence determines the Drain current (I_D).

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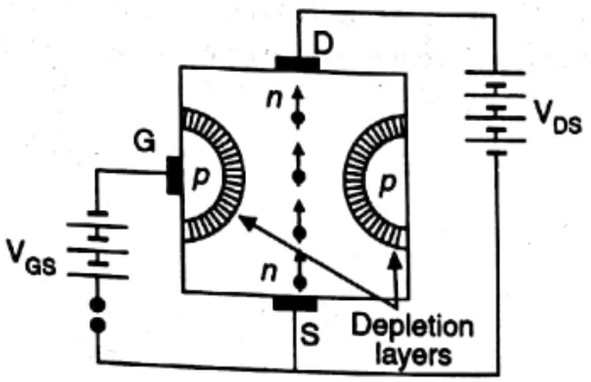


Fig. 2: *Diagram of an n-channel Type FET*

Initially, the Drain current (I_D) increases rapidly with Drain-Source voltage (V_{DS}) but it finally attains a constant value. The Drain Source voltage at which drain current (I_D) becomes a constant is known as Pinch off Voltage. Increase in Drain-Source voltage after this point does not give rise to any increase in drain current (I_D).

When a reverse voltage V_{GS} is applied between the Gate and the Source the width of the depletion layer increases effectively. It decreases the area of cross-section of the available conducting channel and thus increases the resistance. As the resistance of this narrow channel increases the Drain current decreases correspondingly. This can also be stated as the flow of electrons from the Source to the Drain decrease. In this way, the value of Drain current I_D for a given Drain Source voltage (V_{DS}) depends upon the applied Gate-Source voltage (V_{GS}).

As the V_{GS} becomes more negative the value of drain current decreases. Further I_D attains a constant saturation value corresponding to an applied value of voltage V_{DS} which is also known as pinch off voltage.

In this way, we find that the value of Drain current I_D passing from Source to Drain can be controlled by the voltage or the field applied to the Gate. This is the reason why such a transistor is known as a Field Effect Transistor.

If we take a p-channel FET (Refer Figure 3) as shown in the that the negative of the battery V_{DS} is applied to the Source and positive part of the battery VOS is connected to the Gate to make the Gate G at reverse bias with respect to the Source. The electric current goes from S to D but this time the charge carriers are the holes instead of electrons. Thus the charge carriers in a p-channel FET are holes whereas in an n-type channel FET are the electrons. In an FET the current conduction is because of one kind of charge carriers according to its arrangement.

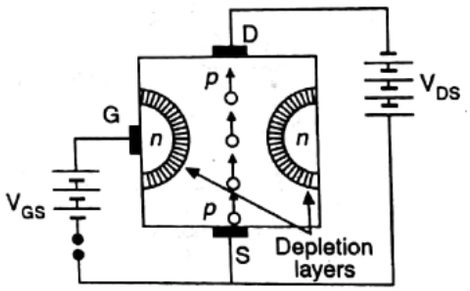
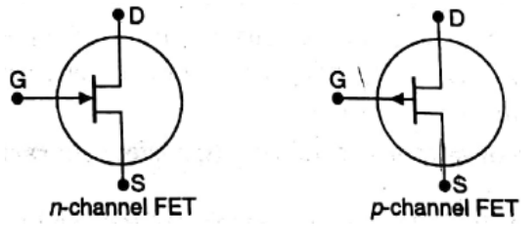


Fig. 3: *Diagram of a p-channel Type FET*

A schematic diagram of an Field Effect Transistor is shown in figure 4. The vertical line represents the channel. The Source and Drain are connected to this line. If the channel is n-type (Refer Figure 4a) the arrow on the Gate is drawn from the Gate to the channel otherwise for a p-type channel (Refer Figure 4b) the arrow is drawn from the channel to the Gate.

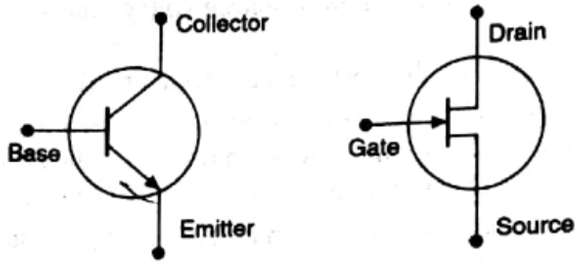


(a) *(b)*

Fig. 4: *A Schematic Diagram of an n-type and p-type Channel Field Effect Transistor*

Comparing a Field effect transistor FET with a Bipolar Junction Transistor BJT we find that

1. The Source, Gate and Drain of an FET corresponds to the Emitter, Base and Collector of a BJT (Refer Figure 5a and 5b).



(a) *(b)*

Fig. 5: *A Schematic Diagram of (a) BJT and (b) FET*

2. Further as the input circuit, i.e., Gate to Source is reverse biased it has a high input impedance whereas the input circuit of a BJT, i.e., Base to Emitter is forward biased and, therefore, has a low input impedance.

NOTES

3. FET is a voltage operated device i.e. input voltage controls the output current on the other hand a BJT is a current operated device i.e. input current controls the output current.
4. Like BJT, the FET can also be used in three basic configurations i.e. Common Source, Common Gate and Common Drain configurations as shown in Figure 6a, 6b and 6c.

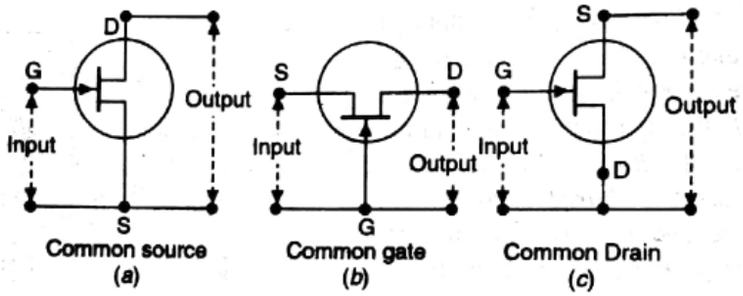


Fig. 6: *A Diagram Representing Common Source, Common Gate and Common Drain Configurations of an FET*

For FET there is a phase shift of pi for common source configuration and there is no phase shift for other two configurations. An FET has a high input impedance as well as a high output impedance.

It is a voltage controlled device and there are only one kind of charge carriers, i.e., electrons in n-type and holes in a p-type channel.

Characteristics of a Field Effect Transistor

(i) Output characteristics, The output characteristics of an FET is the curve between Drain- Source voltage V_{DS} and corresponding Drain current I_D at a constant Gate-Source voltage V_{DS}.

(ii) Transfer characteristics. The transfer characteristics of an FET is the curve between Gate-Source bias (voltage) V_{GS}, and corresponding Drain current I_D at a constant Drain-Source voltage V_{DS}. It is also known as mutual characteristics.

Experiment 1: To observe the Output and mutual characteristics of a Field Effect Transistor.

Apparatus Required: An n-channel FET, D.C. power supply of 0-20 V and 0-12 V, Two voltmeters, a milli-ammeter, two capacitors each of 50 microF (50 V).

Procedure: 1. Draw a diagram showing the scheme of connections as given in Figure 7. and connect them accordingly.

The choice of power supply, voltmeter and milli-ammeter depends upon the characteristics of FET. As electronic power supplies have been used for applying the drain source voltage and gate source bias a capacitor of 50 microF has been connected into each circuit to filter the ripples.

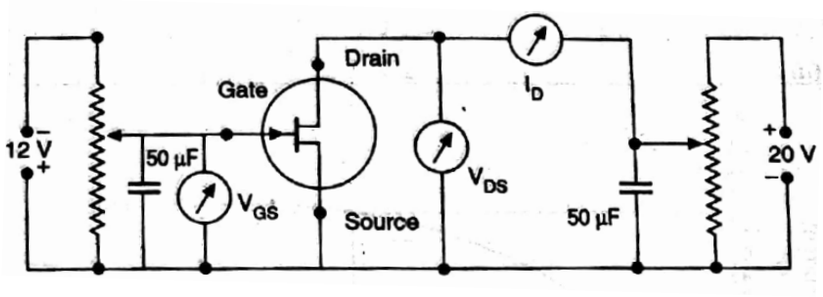


Fig. 7: *A Diagram Showing FET Connections*

2. **Output Characteristics**

   Now keep the Gate-Source bias at l V and again note the values of Drain-Source voltage V_{DS} from zero upwards and corresponding values of Drain current I_D till three constant readings of I_D are obtained.

3. Similarly repeat with a Gate-Source bias of 2V and 3V (or in smaller steps of 0.5 V in each case increasing the Drain-Source voltage V_{DS} from zero upward till three constant values of I_D are obtained.

4. **Transfer Characteristics**. Keep the Drain-Source voltage at +1 volt or at any suitable value in accordance with the data of the FET used. Slowly increase the Gate-Source bias V_{GS} from zero towards increasing negative values in steps of 0.5 to l volt. Note the values of VGS and corresponding values of Drain current I_D. It is seen that as the negative Gate Source bias increases. the Drain current I_D decreases. Hence go on increasing the negative Gate Source bias till the current I_D becomes zero.

5. Similarly repeat with Drain Source voltage of +2 V and +3 V or other suitable values according to FET data.

Observations. (a) Output Characteristics

Sl No.	V_{GS} = 0V		V_{GS} = –1V		V_{GS} = – 2V		V_{GS} = – 3Y	
	V_{DS}	I_D	V_{DS}	I_D	V_{DS}	I_D	V_{DS}	I_D
1.								
2.								
3.								
4.								
5.								
.								
.								
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15.								

NOTES

6. For output characteristics draw graphs between Drain current I_D taken along Y-axis and Drain- Source voltage V_{DS} taken along x-axis for various values of Gate-source voltage V_{GS} on the same graph (Figure 8)

Sl. No.	*Gate Source bias V_{GS}*	*Pinch Off Voltage*
(i)	*OV*	*V*
(ii)	*–1V*	*V*
(iii)	*–2V*	*V*

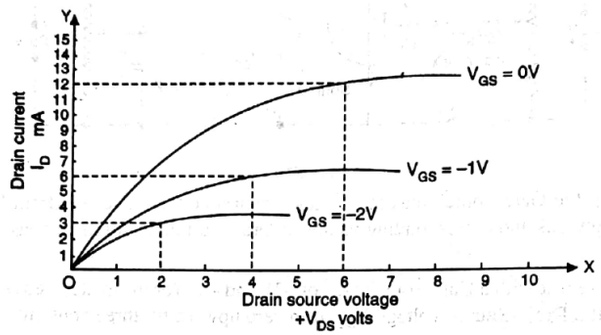

Fig. 8: *An Indicative Curve of Output Characteristics of a FET*

As the value of reverse gate source voltage increases, pinch off occurs at a smaller Drain-Source Voltage (V_{DS}).

(b) Transfer Characteristics or mutual characteristics. [Gate Source bias VGS, Drain current ID graph].

Sl No.	V_{DS} = 3V		V_{DS} = 2V		V_{DS} = 1V	
	V_{GS}	I_D	V_{GS}	I_D	V_{GS}	I_D

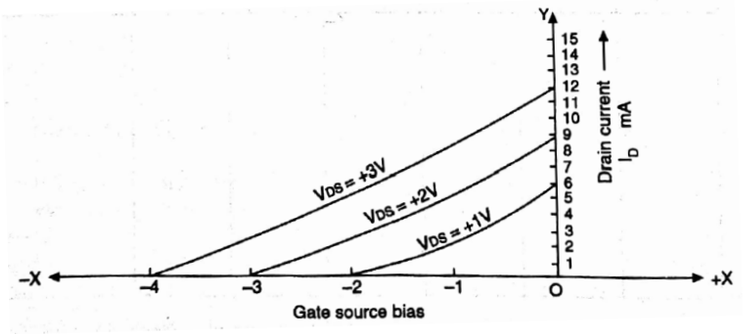

Fig. 9: *An Indicative Curve of Transfer Characteristics of a FET*

7. For transfer characteristics draw graphs between Drain current I_D taken along the Y-axis and V_{GS} Gate Source bias along X-axis as shown m Figure 9.

   Field Effect Transistor

   The end points of the transfer characteristic curves are:

   (1) $V_{GS} = O$ and $I_D = I_{DSS}$ i.e. the maximum saturation value of Drain current.

   (2) $V_{GS} = V_{GS(off)}$ i.e. the value of negative Gate Source bias for which drain current ID is cutoff and $I_D = 0$.

   Note. When the drain current in cut off $V_{GS} = -V_P$ the pinch off voltage. V

   Note the value of I_{DSS} and $V_{DS(off)}$ for different values of V_{DS}.

Sl No.	*Drain Source Voltage (V_{DS})*	*Saturation Drain Current (I_{DDS})*	*Cut off Value of Gate Source bias V_{GS} (Off)*

Precautions

1. Note the maximum rating of FET and the temperature upto which it can be used.
2. Note whether the FET is n-channel or p-channel device and apply the Gate Source bias and Drain Source voltage accordingly.
3. For an electronic D.C. power supply use 50 microF capacitor to stop the ripple.

2. STUDY OF CHARACTERISTICS OF TRANSISTORS (CE MODE)

Introduction

Transistors: Transistor is a semiconductor device capable of amplification in addition to rectification. These are active electronic devices. They are small, require small operating voltage, relatively easy to make at cheaper price. Modern transistors fall into two main classes: bipolar transistor which depend on the flow of minority and majority carries through the devices and unipolar transistors in which current is carried by majority charge carriers.

NOTES

Working

Bipolar Junction Transistors

In a bipolar junction transistor, two p-type semiconductor regions are separated by a thin n-type region, making a p-n-p type structure. Alternatively, in an n-p-n structure a thin p-type region is sandwiched between two n-type regions (Refer Figure 1).

In both, the thin central region is called the base and one outer region is called the emitter and the other is called as the collector. When used as an amplifier, the emitter-base collector-base junction is reverse-biased. The emitter is highly doped and is the source of majority carriers i.e., holes in p-n-p and electrons in an n-p-n type structure. The collector is comparatively lightly doped and collects the carriers. the symbols of the two types of transistors as shown in the figure. The arrow indicates the direction of the current when the emitter base junction is forward-biased.

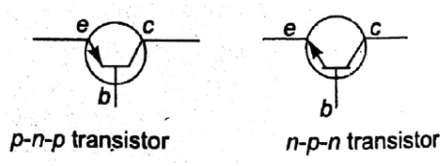

Fig. 1: *Transistors*

Working of an n-p-n-Transistor

Figure 2 shows the n-p-n transistor with forward bias to emitter-base Junction and reverse bias to collector-bias junction. The battery voltage which gives the forward required to be small magnitude whereas the battery giving the reverse bias is or comparatively high value. The forward bias causes the electrons in the emitter to flow toward the base.

This constitutes the emitter current I_E. As the electrons flow from the p-type base, they tend to annihilate with the holes. as the base is lightly doped and very thin only a few electrons combine with the holes (even less than 5%). To replnish the lost holes in p-type base, an electron moves out of the base electrode for each recombination and result in base current I_B. The remaining electrons cross over into the collector region and constitute the collector current I_C. In this way the collector current is closely equal to the emitter current. It is obvious that the emitter current is the sum of base and collector current.

$$\mathbf{I_E = I_B + I_C}$$

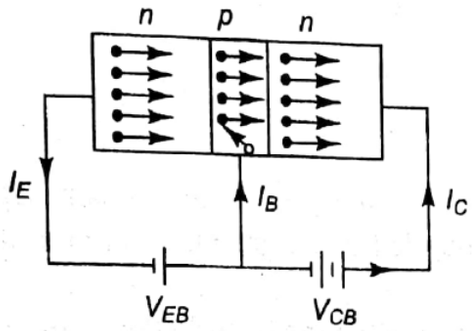

Fig. 2: *The n-p-n Transistor*

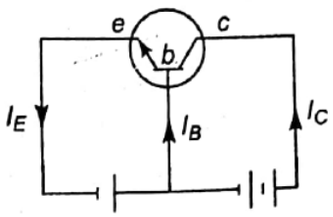

Fig. 3: *The p-n-p Transistor*

Working of p-n-p Transistor

Figure 3 shows the basic connections of a p-n-p transistor. The forward bias causes the holes in p-type emitter to flow towards the base. This constitutes the emitter current I_E. These holes cross through the n-type base, and they tend to combine with the electrons. As these base is lightly doped and very thin, therefore only a few holes (less than 5%) combine with the electrons. To replenish the lost electrons in the n-type base, an electnon moves in the base electrode for each recombination and results in the base current IB. The remaining Holes (more than 95%) cross into the collector region to constitute the collector current I_C. In this way, approximately entire emitter current flows to the collector circuit. Thus the conduction within a p-n-p transistor is by the majority carriers, i.e., $I_E = I_C + I_B$

Importance of Transistor Action

The input circuit (the emitter based junction) has low resistance because of the forward bias whereas the output circuit (the Collector-base junction)-has high resistance due to reversed biased system. As discussed the emitter current almost entirely flows through the collector circuit. In this way, a transistor passes the input current from a low impedance (here it is resistance) circuit to a high impedance circuit. This is responsible for the amplifying action of the transistor.

Transistor Configuration

In an input side to which an input signal is applied and an output side on which an output signal is taken. There may be three common transistor configurations

(i) Common-base

(ii) Common-emitter

(iii) Common-collector

NOTES

The common terminal is connected to the ground and accordingly the above three configurations are also called as grounded base, grounded emitter and grounded collector, respectively.

Each circuit has specific advantage and shortcomings. regardless of the connections the emitter is always bound in forward bias while the collector is always connected in reverse bias.

Experiment 2: To study the common emitter characteristics of a p-n-p junction transistor.

Apparatus Required: A p-n-p transistor, two batteries of 3V and 9V each. A potentiometer of total resistance of 1Mohm and another of the resistance of 25kohm, two voltmeters of range 0-3V and 0-10V and for current measurement, one microammeter (0-200 nA for Ib measurement) are used as shown in Figure 3.

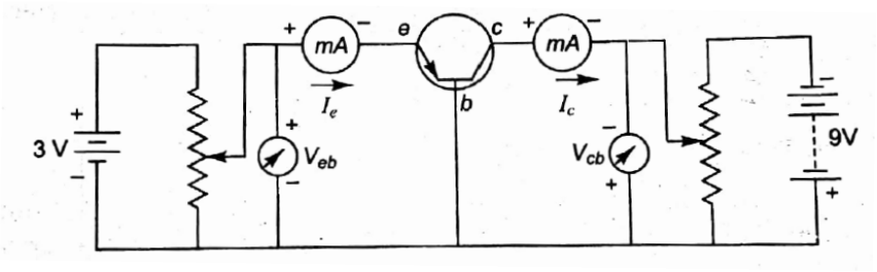

Fig. 4: *Base Diagram of Circuit*

Theory

Input Characteristics

The curve which shows the variation between input current and input voltage for different output voltages are called the input characteristics curves. The input characteristics of a p-n-p transistor are described as the relation between input or base current (I_B) and input or say base-emitter voltage (V_{BE}).

In this case of Common Emitter (CE) configuration, the input current (I_B) is basically produced in the base region which is doped quite lightly and has a very small width as compared to collector and emitter. That is the reason that the base region produces a small input current (I_B). On the other hand, in a Common-Base(CB) configuration, the input current (I_E) is produced in the emitter region which is heavily doped and has a large width, comparatively. As a result, the emitter region produces a huge input current (I_E). Therefore, the input current (I_B) produced in common emitter (CE) configuration is very much small as compared to this common-base (CB) configuration.

The width of the depletion layer at this emitter-base junction is very small on the other hand the width of the depletion layer at the collector-base junction is very large.

If output voltage (V_{CE}) applied to the collector-base junction was further increased, the width of the depletion region increased correspondingly. The base region is lightly doped as compared to the collector region. So the depletion layer penetrates more into the base region. As a consequence, the width of the base region decreases which after all reduces the input current (I_B) produced in this region.

Dynamic Input Resistance (r_i)

The Dynamic input resistance is described as the ratio of change in input or base voltage (V_{BE}) to the corresponding change in input or base current (I_B), when the output voltage (V_{CE}) kept constant.

$$r_i = \frac{\Delta V_{BE}}{\Delta I_B}, \qquad V_{CE} = \text{constant}$$

In CE configuration, the input resistance is low.

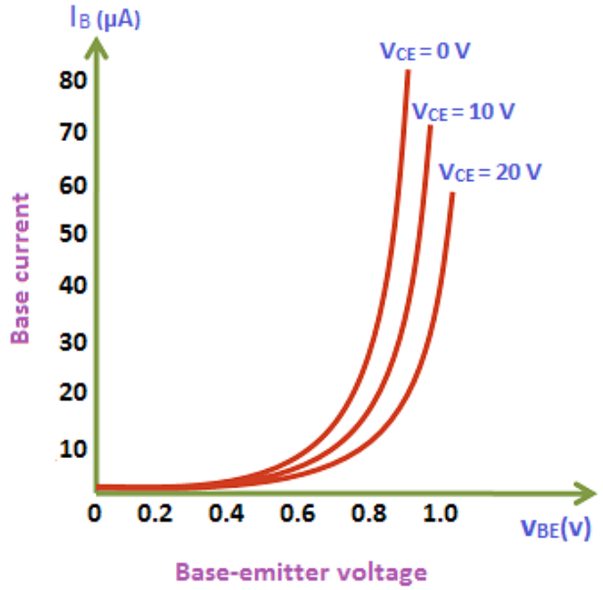

Fig. 5: *I/P Characteristics CE Configuration*

Procedure

1. Connect the circuit as shown in the circuit diagram.
2. The experiment is to determine the input characteristics, in this, the output voltage which is V_{CE} is kept constant and the input voltage V_{BE} is increased from zero to different voltages. For each level of the input voltage (V_{BE}), the corresponding input current (I_B) is recorded.
3. A curve is then drawn between input current I_B and input voltage V_{BE} at constant output voltage V_{CE} (0 volts).

NOTES

4. Increase the output voltage (V_{CE}) from zero volts to a certain voltage level (say 5 or 10 volts) and keep it constant for this reading. While increasing the output voltage (V_{CE}), the input voltage (V_{BE}) should be kept at zero volts. As the output voltage (V_{CE}) kept fix at a constant voltage of 10 volts, the input voltage V_{BE} was increased from zero to a higher voltage at different voltage levels. For each input voltage (V_{BE}), the corresponding input current (I_B) is recorded.
5. A curve is then drawn between input current (I_B) and the input voltage (V_{BE}) at constant output voltage V_{CE} (10 volts). This process was repeated and different curves for fixed values of the output voltage (V_{CE}) was recorded.
6. Take a Cartesian graph and plot X and Y axis. The input or base current (I_B) is to be taken along the y-axis and the input voltage (V_{BE}) is to be taken along the x-axis.

When the output voltage (V_{CE}) is zero volt then the emitter-base junction is obviously at forward bias by the input voltage (V_{BE}). The emitter-base junction acts like a normal p-n junction diode. So the input characteristics of a CE configuration looks same as a normal p-n junction diode characteristics.

The cut-in voltage of a transistor made of silicon is 0.7 V and for germanium, it is 0.3V. In our case, it is made up of silicon. So from the above graph, we can interpret that beyond 0.7 V, a small increase in input voltage (V_{BE}) can increase the input current (I_B) rapidly.

From the above characteristics, we can analyze that for the higher fixed values of the output voltage (V_{CE}), the corresponding curve shifts towards the right side. This is the reason for the higher values of the output voltage, the cut-in voltage increased above 0.7V. To overcome this voltage, more input voltage (V_{BE}) is needed than the previous case.

Output Characteristics

The output characteristics of a transistor are described by getting the relationship between output current (I_C) and output voltage (V_{CE}).

Take output or say collector current (I_C) along the y-axis and take the output voltage (V_{CE}) along the x-axis and plot the output characteristics.

Dynamic Output Resistance (r_o)

Dynamic output resistance is described as the ratio of change in collector voltage (V_{CE}) to the corresponding change in collector current (I_C), when the input current or base current (I_B) was kept constant.

$$r_o = \frac{\Delta V_{CE}}{\Delta I_C}, \qquad I_B = \text{constant}$$

In a CE configuration, the output resistance is high.

NOTES

Procedure

1. Connect the circuit as shown in the circuit diagram.
2. To determine the output characteristics of a transistor, initially, the input or base current I_B is kept constant at 0 µA and the output voltage V_{CE} is increased from zero to higher voltages. For each output voltage, the corresponding output current (I_C) is recorded.

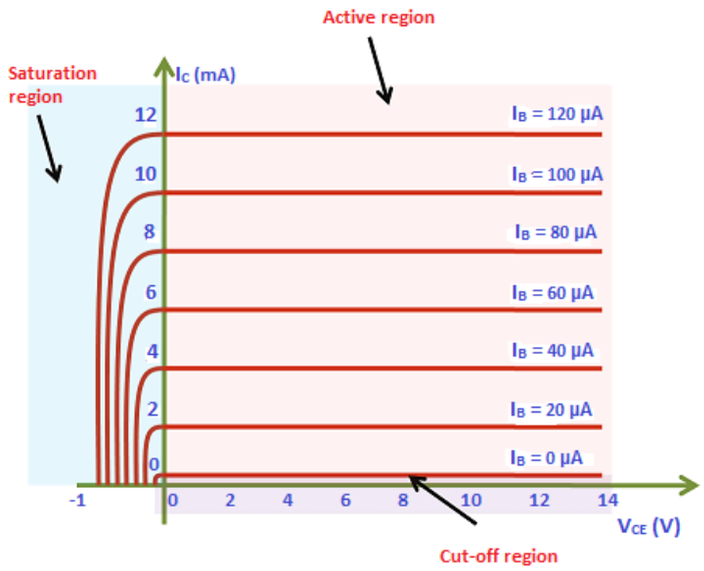

Fig. 6: *O/P Characteristics CE Configuration*

3. A curve between output current I_C and output voltage V_{CE} is then drawn at constant input current (0 µA). When the base current I_B = 0 µA, the transistor works in the cut-off region. In this region, both junctions are reverse biased.
4. Next, the input current (I_B) is increased from 0 to 20 µA by varying the input voltage (V_{BE}). The input current (I_B) is kept constant at 20 µA for this part of the experiment. While increasing the input current (I_B), keep the output voltage (V_{CE}) constant at 0 volts.
5. After the input current (I_B) was kept constant at 20 µA, the output voltage (V_{CE}) is increased from zero to different higher voltages. For each applied output voltage (V_{CE}), the corresponding output current (I_C) is recorded.
6. Now draw a curve between output current (I_C) and output voltage (V_{CE}) at a constant input current of 20 µA. This region is called as an active region of a transistor. In this region, emitter-base junction is at forward biased while the collector-base junction works as reverse biased.
7. Repeat these steps for other higher values of input current (I_B) kept fixed at 40 µA, 60 µA, 80 µA and so on.

When the output voltage V_{CE} is reduced to a very small value such as 0.2 V, the collector-base junction acts as forward biased. This happens because the output voltage V_{CE} has very less effect on the collector-base junction than its input voltage V_{BE}.

As it is well known that the emitter-base junction is in forward biased. So, when both junctions are at forward bias, the transistor works in the saturation region. In this region, a small increase in output voltage (V_{CE}) increases the output current I_C quite rapidly.

Results and Observations

Input Characteristics				
V_{BB} (Volts)	V_{CE} = 0V		V_{CE} =5V	
	V_{BE} (Volts)	I_B (μA)	V_{BE} (Volts)	I_B (μA)

Output Characteristics						
V_{CC} (Volts)	1_B = 0μA		1_B = 20 μA		1_B = 40 μA	
	V_{CE} (Volts)	I_C (mA)	I_{CE} (mA)	I_C (μA)	V_{CE} (Volts)	I_C (mA)

Plot the input characteristics by taking $\mathbf{V}_{BE}$ along X-axis and $\mathbf{I}_B$ along Y-axis for a constant $\mathbf{V}_{CE}$. Similarly, Plot output characteristics by taking $\mathbf{V}_{CE}$ on X-axis and taking $\mathbf{I}_C$ on Y-axis taking $\mathbf{I}_B$ as a constant.

Calculations from Graph

1. **Input Characteristics:** To obtain the input resistance of an input characteristic, first find ΔV_{BE} and ΔI_B for a constant $\mathbf{V}_{CE}$ on any of the input characteristics.

   Input impedance = $R_i = \Delta \mathbf{V}_{BE} / \Delta \mathbf{I}_B$ ($\mathbf{V}_{CE}$ is Constant)

   Voltage gain = $\Delta \mathbf{V}_{EB} / \Delta \mathbf{V}_{CE}$ ($\mathbf{I}_B$ = Constant)

2. **Output Characteristics:** To find output resistance get $\Delta \mathbf{I}_C$ and $\Delta \mathbf{V}_{CB}$ for a constant base current $\mathbf{I}_B$.

Output admittance = $R_o = \Delta I_C / \Delta V_{CE}$ (I_B is Constant)

Current gain = $\Delta I_C / \Delta I_B$ (V_{CE} = Constant)

Precautions

1. While performing the experiment does not exceed the safe voltage rating of the transistor. This may lead to a permanent damage to it.
2. Voltmeter and Ammeter must be connected in correct polarities as given in the circuit diagram.
3. Do not switch the power supply ON until you have checked the circuit connections according to the circuit diagram.
4. Make sure while picking the emitter, base and collector wired terminals of the transistor.

3. STUDY THE CHARACTERISTICS OF A ZENER DIODE AND CONSTRUCT DC POWER SUPPLY

Introduction

The Zener diode is a general-purpose diode which is used to regulate voltage. When a Zener diode is biased in the forward direction then it behaves like an ordinary diode. In case a reverse voltage is applied to it, the Zener diode works in a different way and the voltage remains constant for a broad range of current.

Avalanche Breakdown: There is obviously a limit for the reverse voltage. The applied Reverse voltage can be increased only until the diode breakdown reaches. The point where this happens is called *Avalanche Breakdown*. At this stage, the diode behaves like a short circuit and the maximum current will flow through the Zener diode.

Theory

The use of Zener Diode is basically in its "reverse bias". From the given I-V Characteristics curve, one can study that the Zener diode in its reverse bias characteristics shows a region where it regulates almost a constant negative voltage regardless of the quantity of current flowing through it. The applied reverse voltage remains nearly constant even when large changes in current happen. The Zener diodes works till the current remains less than the breakdown current.

This ability to control voltage by itself can be used to regulate or stabilize a voltage source against a power supply. Using the fact that the voltage across the diode in its breakdown region remains constant, an important application of the zener diode as a voltage regulator can be derived.

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Characteristics: Here Figure 1 shows the current Vs voltage curve for a Zener diode. The characteristics are almost the same as a normal diode in case of forward bias. One can observe the nearly constant voltage in the breakdown region.

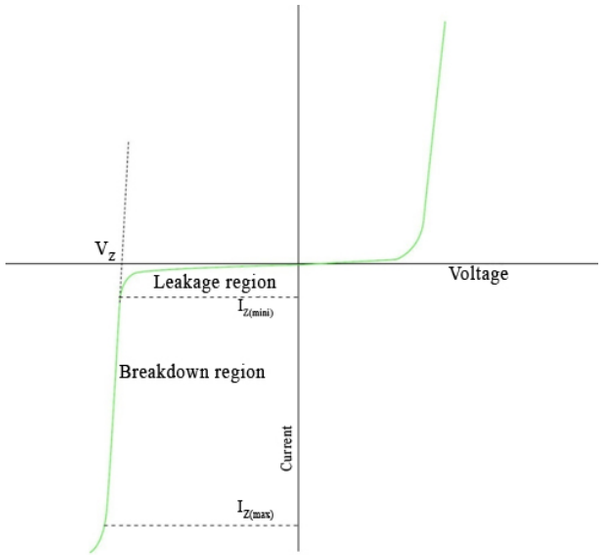

Fig. 1: *Typical Zener Diode Characteristics*

As mentioned earlier that the forward bias characteristics of a Zener diode are identical to that of a regular diode. The threshold forward voltage with a current of around 1 mA is around 0.6 volts, at room temperature. In the case of reverse bias, Zener diode behaves like an open circuit with only a small leakage current (because of impurities) is flowing as shown in the plot. As the applied reverse voltage increases, the breakdown voltage is approached and the current will begin to avalanche. The initial transition from leakage to Zener voltage is soft but then after the current increases quickly as drawn in the plot. The characteristics reveal that the voltage across the Zener diode in this breakdown region is almost constant. There is only a small increase in voltage with a huge amount of increasing current. At a level, when the quantity of current passing by is quite high, the power dissipation of the diode becomes very large and the diode is destroyed by the heat. There is required a minimum Zener current, $I_{(min)}$, that is necessary to places the operating point in the desired breakdown region. There is also a maximum Zener current, $I_{(max)}$, at which the power dissipation takes the junction temperature to the maximum allowed value. Beyond that, the diode can be damaged.

Zener Diode as a Voltage Regulator

The main function of a regulator is to provide a constant voltage to the load connected in parallel. The load must be independent of the ripples in the main supply voltage or any variation in the load current. Zener diode will

continue to provide a constant voltage until the diode current falls between the minimum $I_{(min)}$ value or the maximum current I_{max} causing breakdown in the reverse breakdown region. It permits the current to flow in forward direction as usual, but will allow it to flow in the reverse bias when the voltage is above a certain value. Zener diode is made specially to have a breakdown at a specific reverse voltage. Otherwise its characteristics are very similar to a common diode. In reverse the voltage through the Zener diode is almost constant over a wide range of currents makes it useful as a voltage regulator.

The main purpose of a voltage regulator is to maintain a constant supply of voltage across a load irrespective of the variation in the applied voltage and variations in the load current. A Zener diode as a regulator is shown in the Figure 2. For all the combinations of input voltage and load current the Zener diode passes the excess current and maintains a constant voltage across the load. The Zener conducts the minimum current when the load current is the highest and it conducts the maximum current when the load current is the lowest.

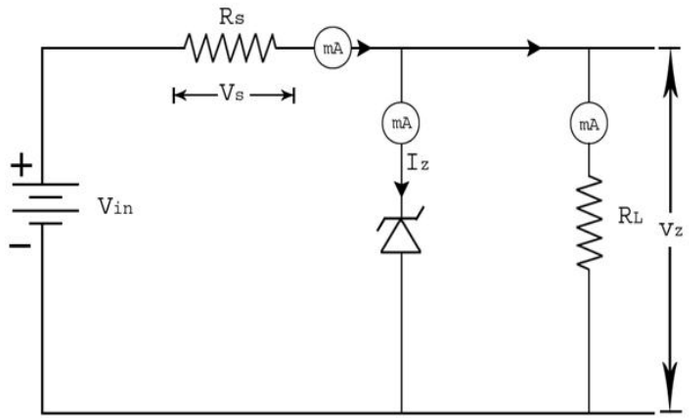

Fig. 2: *Zener Diode Used as a Voltage Regulator*

In the case when there is no load resistance, the shunt regulator can be used to dissipate the total power passing through the resistance in series and the Zener diode has an inherent current limiting advantage under the conditions when there is a fault in the load because then the resistor in series limits excess current.

A Zener diode of break down voltage (V_B) is connected in reverse to an input voltage (V_i) across a load resistance (R_L) and a resistor in series (R_S). The voltage across the diode will remain constant at V_B for all the values of Zener current (I_Z) as long as the current remains in the breakdown region. Hence a regulated DC output voltage $V_0 = V_Z$ is obtained across the load resistance (R_L), whenever the input voltage remains within a range of operating voltage.

Experiment 3: Study the characteristics of Zener diode and construct regulated DC power supply

Apparatus Required: Zener diode, resistor, variable DC power supply, milli-ammeter, a voltmeter, Rheostat, and some connecting wires.

Procedure

1. Connect the circuit as given in the above diagram (Refer Figure 3).
2. First, make readings in reverse bias mode. For that, slowly increase the reverse bias voltage in small steps. While doing all this, keep noting down the readings of the ammeter and the voltmeter.
3. There are two ammeters in the diagram, the first one is connected in series with the Zener diode and another one is connected in series with the load resistance of 3.3 kΩ. Let's call them A_1 and A_2, respectively. After a particular value of applied reverse bias voltage, the value of current in A_1 will suddenly blow up.
4. Note down the ammeter and voltmeter reading at this point. This voltmeter reading is Zener breakdown voltage. Keep increasing the voltage further. We will see that the voltage across the Zener diode remains constant. On the other hand, the current through it is continuously increasing. Note down the different values of the current and voltmeter at reverse bias. Tabulate the values of current and voltage in the given table.

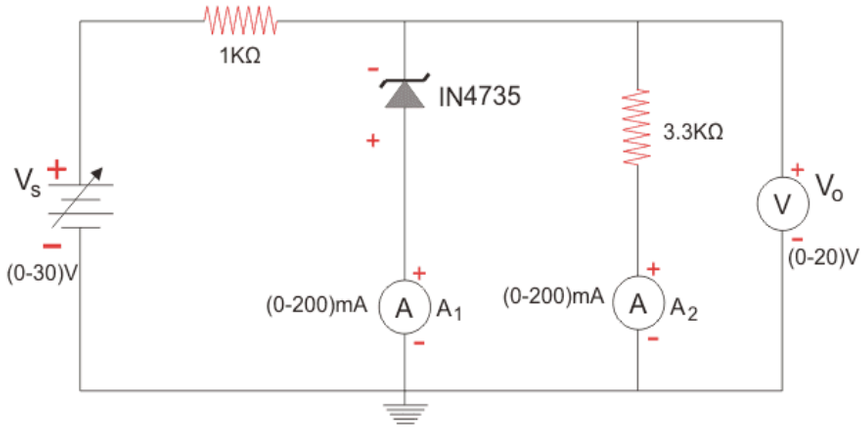

Fig. 3: *A Schematic Diagram of a Zener Diode as a Voltage Regulator*

5. Now, perform the same experiment by connecting the Zener diode in the forward bias. Note down the current and voltage readings for all applied voltages.

NOTES

Table 1: *A Table of Observation of Zener Diode*

Sr. No.	Input Voltage	Output Voltage	Current in A1	Current in A2

6. The table of observation should look like the one shown above (Table). Draw this table two times once for the forward and once for the reverse bias. Put these values in the table. Draw the I-V graph corresponding to these values in a single plot. This is the characteristic curve of the Zener diode.
7. Note down the particular value at which the value of current increases rapidly in case of reverse biased mode. This voltage is known as Zener breakdown voltage.

Precautions

1. Different Zener diodes may have different breakdown voltages. A Zener diode must be selected whose breakdown voltage is less than the voltage of the input voltage source.
2. While doing this experiment, choose the voltmeter and ammeter of a range in which many points can be taken over breakdown region.
3. Voltage after a certain value may damage the Zener diode.

4. CONSTRUCT THE LOGIC GATES USING DISCRETE COMPONENTS

Introduction

A logic gate is a physical device implementing Boolean function; such that it performs logical operations on one or more binary inputs and they produce a single binary output as a result. There are many readymade ICs available in the market to get these gates on demand but for the purpose of learning, it is important to understand the structure and functioning of these gates using their individual components.

There is one more reason to learn this is that you don't need dedicated IC's for each gate but you can make these gates by basic available components.

NOTES

for an example if all you need is an AND gate, to reset a counter. Then it can be easily implemented with two diodes and one resistor. You don't need a whole additional IC such as 7400, containing four AND gates, of which only one is needed. At other times, it is also convenient to construct a logic gate with as many inputs as you like. For example, a 7 point input OR-gate can be easily implemented by adding more diodes to the basic two-input gate. You might not have the required IC's, but you can always have some resistors and some diodes. So, this is an another reason for using logic gates made from their discrete components.

There are also some disadvantages to these logic gates made by discrete components. The most noticeable discomfort is that the output current ability of these gates is quite low. It is generally determined by the resistors used in construction. This also depends upon the current handling ability of the gates. In case, the logic gate made out of discrete components are used to drive a high impedance IC input, then there is no problem. If a voltage drop of 0.7V across the diode happens, it means that you cannot flow the simple component based logic gates. This is because you may easily alter the input voltage level needed for a boolean logic to decide its state. The voltage will sink below the level what is recognised as a boolean "1". At the end, the discrete component implementation of logic gates might be improper than their "proper" ICs. But they save the time the need of end ICs in case of simple experiments.

Theory

OR Gate - "OR" gate is one of the easiest gate to understand. There is an easy way to make understanding over the operations of these gates is to take these diode as simple switches, which are closed when the potential at one side (from the anode) is higher than the other end (the cathode). In this way, the current flows in the direction of the arrow. In the given diagram, the symbol, discrete component implementation and the truth table of an OR gate are given.

In an OR gate, the value of output is "1" (high) if either of the inputs is "1" (high). According to the given diagram, if any of the given inputs has a high voltage, then its diode will conduct forwardly and the current will flow to the output. A voltage will be developed across the 10 Kohm resistor, which is equal to the input voltage minus 0.7V (Voltage drop across a silicon diode). On the other hand, If both of these inputs are low "0", then the diodes are reverse biased and don't conduct. hence gives a low signal.

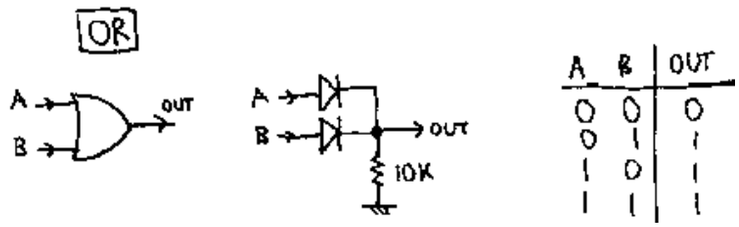

Fig. 1: *Symbol, Circuit and Truth Table of an "OR" Gate*

AND Gate

AND gate is quite similar to the OR gate except the orientation of the diodes. The output of an AND gate is "1" (High) in case when both of its inputs are "1" (high). In this diode-resistor implementation, if any of the input is "low" (which is logically "0") then the potential difference make a forward bias diode and it will conduct. The output is effectively shorted to the ground. In one case when both of the input voltages are "high" (logically "1") then none of the diodes will be in the condition to conduct. This is the reason, the output is not shorted to the ground: it remains at +5V (high) via the given resistor. These are the desired AND gate results. Due to the presence of silicon junction diodes, the actual "low" output signal is 0.7V higher than that of "low" input voltage.

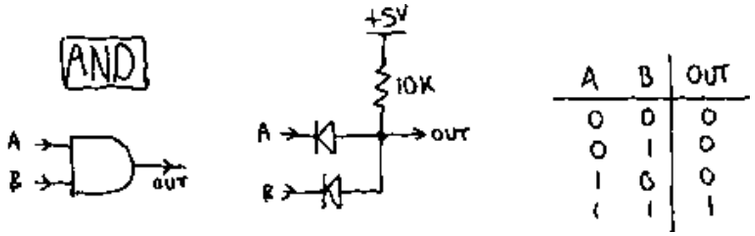

Fig. 2: *Symbol, Circuit and Truth Table of an "AND" Gate*

NOT Gate (Inverter)

Any inverting function can't be done only with diodes and resistors alone. A transistor is also needed, to implement the inverting action. There's nothing predominantly special about the transistor. In such cases, almost any small signal transistor (NPN) will be okay because it is to be driven into the saturation state (unbiased). If the voltage applied to the base of the transistor is more than 0.7V and the transistor will conduct which results in the output to "0", which is low voltage. If the input voltage is "0", the transistor does not conduct in this case, and the resistor will just give the output of +5V. The 10K resistor is always needed as a limiting resistance in the base, otherwise, the excessive base-emitter current may damage the transistor.

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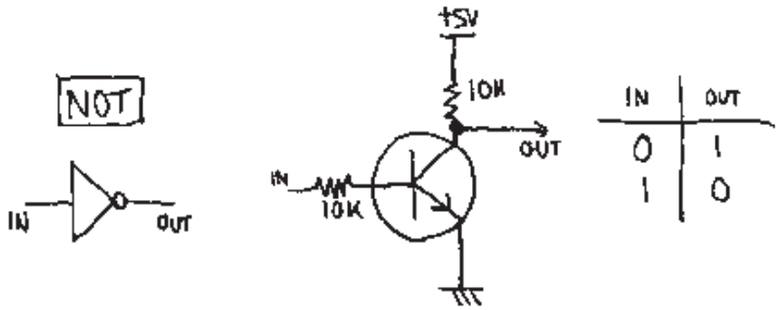
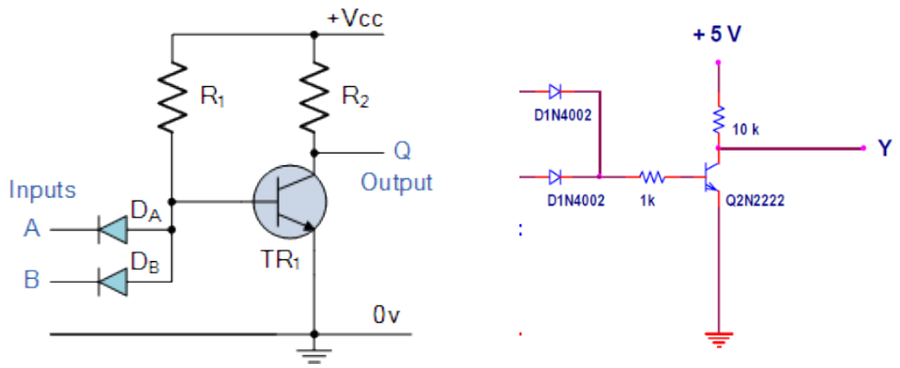


Fig. 3: *Symbol, Circuit and Truth Table of an "NOT" Gate*

NAND and NOR Gates

The construction of NAND and NOR gate is easy. What to do is just use a general AND or OR gate followed by a NOT gate to invert its output. In case, when NAND gate is used, the base resistor of the transistor can be excluded just because the maximum current passing through the system is limited by the 10K resistor in the AND gate.



(a) *(b)*

Fig. 4: *Symbol, Circuit and Truth Table of (a) "NAND" Gate and (b) "NOR" Gate*

XOR Gate

The XOR gate is a little more complicated as compared to the gates given above. Check out the structure and outcomes of an OR gate. In comparison to an XOR gate, an OR gate works for the three of the possible four states in the truth table. The fourth state is odd in which the outcome is 1 when both the inputs are 1. So a way is needed to mold the output to zero. This can be accomplished by using the transistor as a switch, where its base is driven by an AND gate on 2 inputs. When both the inputs are high, an AND gate will activate the transistor, which turns the output to logic "0". Consequently, the XOR gate can be taken as an ordinary OR gate, with an AND gate, and a switch to nullify the output. The extra diode in the base of the transistor

creates an additional 0.7V voltage drop. In absence of this, the 0.7V of the AND gate output would be enough to put the transistor into little conduction.

NOTES

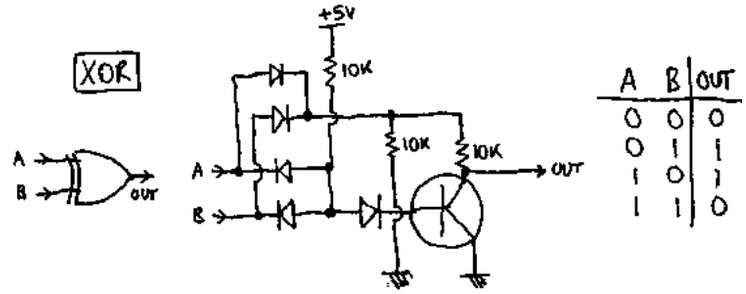


Fig. 5: *Symbol, Circuit and Truth Table of a "XOR" Gate*

Experiment 4**:** Construct the logic gates using discrete components

Apparatus Required: A bread board, Three 10 Kohm resistor, five pn junction diodes, an NPN transistor, some connecting wires, a constant voltage source of 5 V.

Procedure: 1. Make the required circuit diagram of "OR" gate (Figure 1) with their respective components using connecting wires. Similarly construct other gates (Figure 2-5) to verify the truth table.

2. Input all combinations of digital 0 and 1 ("A" : "0" and "1" for not gate and "AB" : "00", "01", "10", "11" for others). And observe the logic signal in the output.
3. Constructing the truth tables.

   Truth table for AND gate

Input A	Input B	Output A.B
0	0	
1	0	
0	1	
1	1	

   Truth table for OR gate

Input A	Input B	Output A+B
0	0	
1	0	
0	1	
1	1	

NOTES

Truth table for NOT gate

Input A	Output A
0	
1	

Truth table for NAND gate

Input A	Input B	Output A.B
0	0	
1	0	
0	1	
1	1	

Truth table for NOR gate

Input A	Input B	Output A.B
0	0	
1	0	
0	1	
1	1	

Truth table for XOR gate

Input A	Input B	Output A.B
0	0	
1	0	
0	1	
1	1	

There are the required truth tables obtained by the gates constructed by the descrete components.

Precautions

1. The 10K resistor has been shown for the purposes of illustration only. In fact the value of the resistance needs to be chosen carefully depending upon the input resistance of the given circuit that needs to be observe the output.
2. Take care of the loose connections in a bread board. The ends of the inserting wires should be conducting properly.

NOTES

5. DESIGN OF FET AMPLIFIER - COMMON SOURCE CONFIGURATION

Introduction

Three terminal devices, such as FET or transistors can be used to install a controllable current source. This property makes them active devices in electronics and just because of this property they are suitable to be used as amplifiers. A p-n-p or n-p-n transistor is an common example of such a device. In particular, FET (Field-Effect Transistor) is a widely used device with three terminals. The working principle of a FET is controlling the flow of current through drain by setting the voltage between gate and source.

A common source FET amplifier is one of the basic single stage field-effect transistor based amplifier. These amplifiers are generally used as a voltage or trans-conductance amplifiers. The Common Source (CS) Field Effect Transistor (FET) amplifier circuit is one of the most frequently used amplifier providing current and voltage gain along with a suitable input/output impedance. The configuration of common source FET is probably used the most because of its circuit configuration for many applications. And also It provides a high level of versatile performance.

The common source FET circuit provides moderate input and output impedance values. Both the current and voltage gains can be explained as moderate, but the output is at 180^{o} phase difference or say the inverse of the input signal. This provides a good all round performance and it is often considered as the most used configuration.

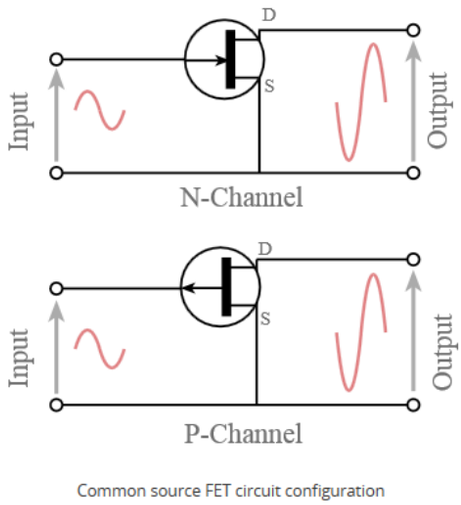


Fig. 1: *A Diagram of CS-FET Amplifier*

Theory

A Common Source - Field Effect Transistor (CS-FET) amplifier is an inverting amplifier which is commonly used for a variety of applications. Its name "common source" comes from the fact that when the source terminal is grounded, it becomes a common terminal for both drain and source terminals. The circuit given below is a typical common source amplifier with a bias and with the coupling and the bypass capacitors. The configuration is somehow same as the common emitter transistor amplifier.

When an AC signal is coupled into the gate, then it produces variations in gate source voltage. This as a result produces a sinusoidal drain current just because an AC current flows through the drain resistor. An amplified AC signal is obtained at the output. A further increase in gate source voltage generates more drain current, which indicates that the drain voltage is decreasing. As the positive cycle of input voltage produces the negative cycle of output voltage, we get a phase inversion in a CS amplifier.

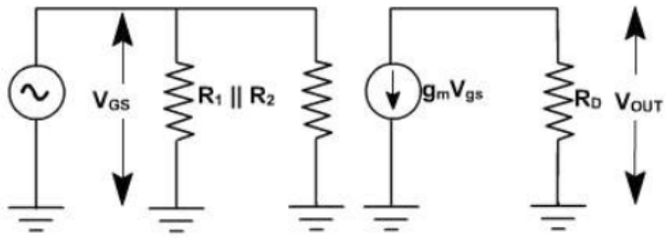


Fig. 2: *AC Equivalent Circuit of a CS-FET*

The AC output voltage is,

$$V_{out} = -_{gm} V_{gs} R_D$$

Here the negative sign means a phase inversion. This is because the AC source is directly connected between the gate source terminals and therefore AC input voltage is,

$$V_{in} = V_{gs}$$

Then the voltage gain is given by,

$$A_v = V_{out}/V_{in} = -g_m R_D = \text{Voltage Gain}$$

Experiment: Design and run a Common Source-Field Effect Transistor amplifier at different frequencies and calculate the value of its voltage amplification (gain) and frequency response.

Apparatus Required: Oscilloscope, DMM, Transistors, FET BFW 11, Resistors of different values, Resistors of 8.2kΩ, 4.7kΩ, 470Ω, and 100Ω values, Capacitors - 100 μF and 2 of 10μF, power supply, function generator.

NOTES

Procedure

1. Connect the circuit as given in the diagram (Refer Figure 3).
2. Apply a sine wave input signal of around 20mv from a signal generator.
3. Connect the output to the DSO.

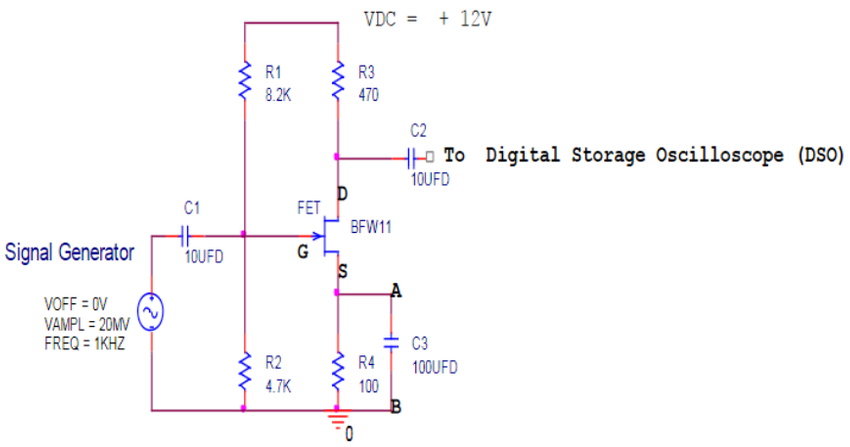


Fig. 3: *Circuit Diagram*

4. Measure output voltage and calculate gain.
5. Keeping the input voltage constant vary the input frequency and note the output voltage of the Amplifier till the output start decreasing.
6. Draw a graph between input frequency vs. output voltage (or gain).

Observation Table

Vin = ... mV

Sr. No.	Input Frequency	Output Voltage (Vout)	Gain (Vout/Vin)

Result

1. Voltage Gain .....
2. Lower cut off Frequency .....
3. Upper cut off Frequency .....
4. Bandwidth .....

NOTES

Precautions

1. Make sure about the gate source terminals of a FET to place it correctly.
2. Make circuit correctly as it is given in the diagram.
3. All the connections should be right and properly tight.
4. All the readings should be taken carefully.
5. Scale on the graph on DSO should be taken correctly and carefully.

6. CHARACTERISTICS OF UNIJUNCTION TRANSISTOR

Introduction

The **Unijunction Transistor** (**UJT)** is a three terminal device that can be used in gate pulse, trigger generator and timing circuits applications to switch and control either by being thyristors or triac for AC power control applications.

Unijunction transistors (UJT) are made from separate p- and n-type semiconductor materials forming a single (hence its name Uni-Junction) pn-junction within the main conducting n-type channel, like diodes. Although UJT has the name of a transistor, but its switching characters are very different from those of a conventional bipolar transistor or field effect transistor (FET). It can not be used to amplify a signal but it can be used as a ON-OFF switching transistor. UJT's have uni-directional conduction and negative impedance character acting more like a voltage divider during its breakdown.

Theory

Similar to n-channel FET, UJT consists of a single piece of n-type semiconductor forming the main current carrying channel with its two external connections named as *Base2* (B_2) and *Base1* (B_1). In this, the third wire, marked as the *Emitter* (E) is located along the channel. This terminal is presented by an arrow pointing from the p-type emitter to n-type base.

The rectifying pn-junction of the UJT is formed by fusing the p-type material into the n-type channel. Moreover, p-type UJT's with an n-type Emitter terminal are also available. This junction is situated along the channel so that it is closer to another terminal B_2 than being close to B_1. An arrow mark is used in the UJT which in fact points towards the base. It indicates that the Emitter terminal is positive while the silicon bar is at negative potential. The Figure below shows the symbol, construction and circuit of a UJT.

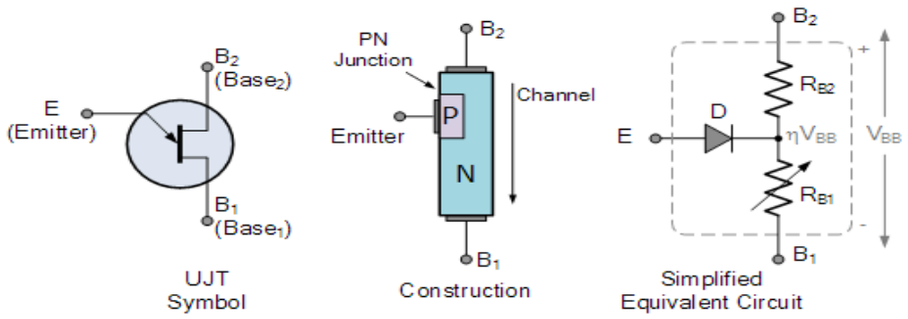


Fig. 1: *Uni-Junction Transistor Symbol and Construction*

It can be notice that the symbol for the UJT looks very similar to that of Junction Field Effect Transistor (JFET), but as a difference it has a bent arrow representing the input which is the Emitter(E). And also, it should be added that JFET's and UJT's work very differently and should not be confused.

So, the matter of the discussion is that how does a UJT work? From the equivalent circuit given above, we can see that the n-type channel is basically contains two resistors, which are R_{B2} and R_{B1} in series with an ideal diode, D represents the p-n junction connected to the center point. This Emitter p-n junction is fixed in position along with the ohmic channel at the time of manufacturing and therefore can not be changed.

Resistance R_{B1} is placed between the Emitter (E) and the terminal B_1, while resistance R_{B2} is given between the Emitter (E) and terminal B_2. As the p-n junction is physically placed closer to the terminal B_2 than B_1, hence the resistive value of R_{B2} will be less than R_{B1}. The overall resistance of the silicon bar will be dependent on the semiconductor's actual doping concentration and the physical dimensions of the n-type silicon channel and it can be represented as R_{BB}. If the resistance is measured with an ohmmeter, the static resistance would typically measure somewhere between 4 to 10 kΩ for commonly available UJT's.

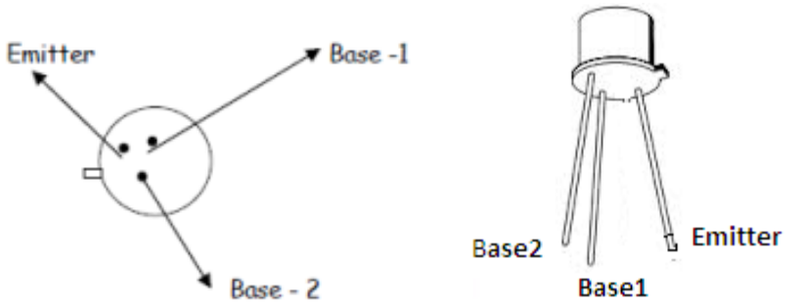


Fig. 2: *Pin Assignment of UJT*

The mentioned two series resistors produce a voltage divider network between two base terminals of the UJT and since this channel goes from

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B_2 to B_1. Whenever a voltage is applied across this device, the effective potential at any point along the channel will be proportional to its distance from any of the terminals which are either B_2 or B_1. And also the value of the voltage gradient will depends upon the amount of the voltage applied.

When it is used in a circuit, the terminal B_1 is connected to the ground and the Emitter serves as an input to the device. Let us consider a voltage V_{BB} is applied across the UJT between the terminals B_2 and B_1 such that B_2 is biased positive relative to B_1. With zero Emitter input, the voltage developed across resistor R_{B1} (the lower resistance) of the resistive voltage divider can be calculated as given by the formula below:

Unijunction Transistor R_{B1} Voltage:

$$V_{RB1} = \frac{R_{B1}}{R_{B1} + R_{B2}} \times V_{BB}$$

For a UJT, the ratio of R_{B1} to R_{BB} shown above is called as **intrinsic stand-off ratio** and it is represented by the Greek symbol: **η** (eta). The typical standard values of η ranges from 0.5 to 0.8 for commonly available UJT's. In case, a small positive input voltage is applied, which is somewhat less than the voltage developed across resistor, R_{B1} (ηV_{BB}) is now applied to the input terminal (Emitter), the diode is reverse biased, thus it offers a very high impedance and the device is not able to conduct. As a result UJT is switched "OFF" and the current flows is zero.

However, when the Emitter input voltage increases and it becomes greater than that value of V_{RB1} (ηV_{BB} + 0.7V, where 0.7V equals the pn-junction diode voltage drop) the pn-junction becomes forward biased and in this case UJT begins to conduct. The Emitter current, ηI_E now flows from the Emitter to the Base. The effectiveness of the extra Emitter current flowing into the Base, as a result reduces the resistive portion of the channel between the Emitter and the B_1 terminal. This reduction in the resistance value (R_{B1}) decreases current to a very low value. That means, the Emitter junction becomes even more forward biased in this case and results in a larger current flow.

Like this, if a applied voltage between the Emitter and the terminal B_1, decreases to a very small value below the breakdown, the value of resistance (R_{B1}) effectively increases to a very high value. In that case, the UJT can be used as a voltage breakdown device. In this way, we can see that the resistance presented by R_{B1} is variable and it is also dependant on the value of Emitter current, I_E. Then in case of the forward biasing, the Emitter junction with respect to B_1 causes more current to flow between the terminals E and B_1. It can also be said that the flow of current into the Emitter decreases the resistive value of R_{B1} and the voltage drop across it, V_{RB1} also decreases, allowing more current to flow.

By now, it is well know that how a UJT works, and for what they can be used. The most common application of a UJT is to trigger a device but other UJT applications include the generation of sawtooth waves, simple oscillators, and timing circuits. One of the simplest UJT circuits is the Relaxation Oscillator producing non-sinusoidal waveforms. In a basic UJT relaxation oscillator circuit, the Emitter terminal of the UJT is connected to the junction of a series resistor and capacitor, RC circuit as discussed in the next experiment.

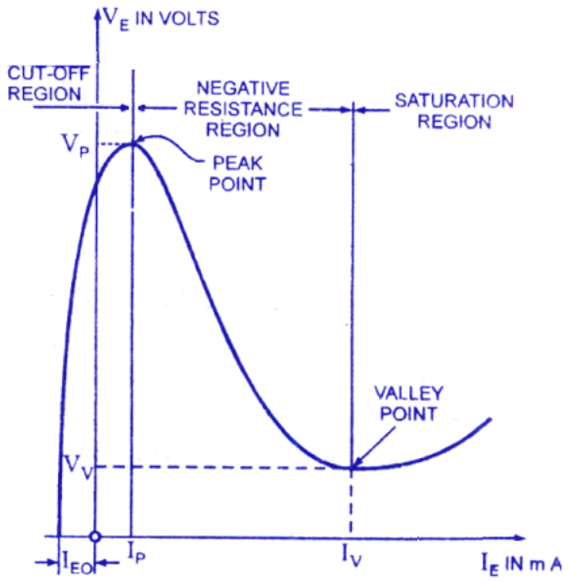

Fig. 3: *An Expected Curve between I_E and V_E*

Experiment: To observe the characteristics of UJT and calculate the Intrinsic Stand Off Ratio(η).

Apparatus Required: Regulated Power Supply (2) (from 0 to 30V, 1A), UJT 2N2646, Resistors of 10kΩ, 47Ω, 330Ω values, a multimeter, a breadboard and some connecting Wires.

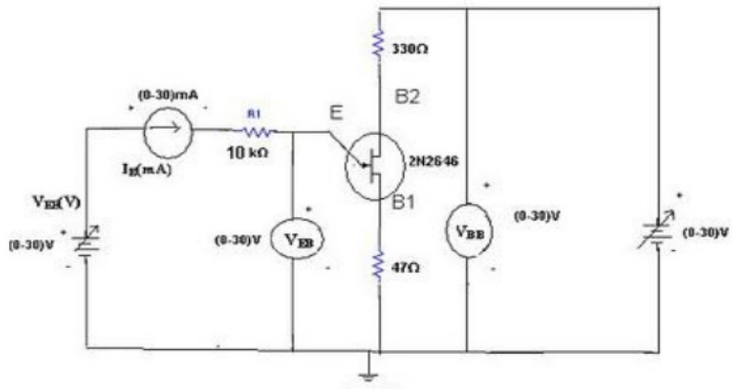

Fig. 4: *The Circuit Diagram to Observe UJT Characteristics*

Procedure

1. Make the circuit connections on a bread board as given in the diagram.
2. Fix the output voltage at a constant level and note down the emitter current values by varying input voltage.
3. Repeat this process for different set of output voltage values.
4. Write all the readings in the table and make a plot with I_E on X-axis and V_E on Y-axis.

   Off ratio is calculated using:

   $\eta = (Vp\text{-}V_D) / V_{B2B1}$
5. Plot a graph between V_E and I_E for different constant values of $V_{B2B1.}$

V_{B2B1} = 2V		V_{B2B1} = 3V	
V_{EB}(V)	I_E(mA)	V_{EB}(V)	I_E(mA)

Calculation

$$V_P = \eta V_{B2B1} + V_D$$

$$\eta = (V_P - V_D) / V_{B2B1}$$

$$\eta = (\eta_1 + \eta_2) / 2$$

Application: UJT can be used as trigger device for SCR's. Triacs and other applications including sawtooth generator, phase control and timing circuits.

Result

The emitter characteristics of UJT are studied as follows:

a. Peak Voltage, V_p _____ Volts.
b. Peak Current, I_p _____ mA.
c. Valley Voltage, V_v _____ Volts.
d. Valley Current, I_v _____ mA.
e. Negative Resistance _____ Ohms.

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Precautions

1. The terminals emitter, Base-1, Base-2 terminals of UJT must be confirmed before putting them in the circuit.
2. Applied voltage should not be more than the listed value of UJT. This may lead to the permanent damage of the UJT.
3. Connect the voltmeter and ammeter in correct polarities as given in the circuit diagram.
4. Do not switch ON the power supply unless you have checked the circuit connections properly.

7. RELAXATION OSCILLATOR (UJT)

Introduction

UJT relaxation oscillator is an RC oscillator where the main active element is a UJT (Unijunction Transistor). UJT is an excellent switch with very small switching time of the order of some nano seconds. It also has a negative resistance region in its characteristics and this can be easily employed in relaxation oscillators. The UJT based relaxation oscillator is called so because the timing interval can be established by the charging of a capacitor and the time interval is ceased by its rapid discharge.

Theory

When a voltage (Vs) is applied to the unijunction transistor (UJT), initially it is "OFF" and therefore the capacitor C_1 has no charge. However, after that it begins to charge exponentially through the resistance R_3. As the emitter, E of the UJT is connected to the capacitor, once the charging potential becomes V_c across the capacitor, it becomes larger than the diode voltage drop, the p-n junction behaves as a standard diode and becomes forward biased triggering the UJT into a conductor. In this case the unijunction electronic transistor is "ON". At this time the emitter to B_1 resistance collapses because the electrode goes into a state of saturated resistance and emitter current flows through R_1.

As the resistance of R_1 is quite low, the capacitor discharges very fast through UJT and a quick rising voltage pulse seems across R_1. Also, as a result the capacitor discharges very fast through the UJT than it will charge up through electrical resistance R_3. The discharging time could be a lot but it is quite fast as it discharges through the low resistance UJT.

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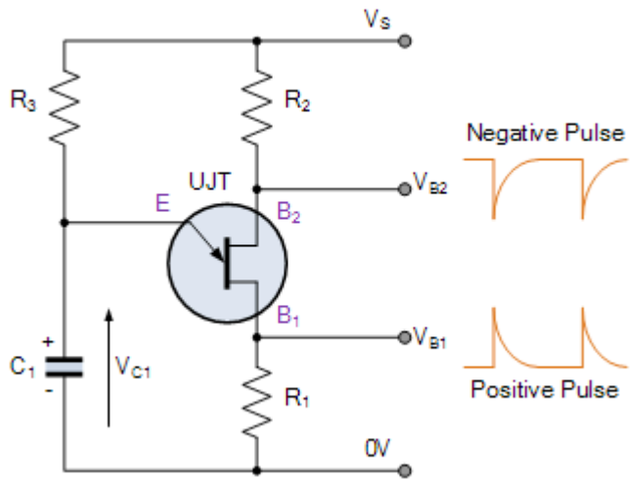

Fig. 1: *Circuit Diagram*

When the voltage across the capacitor decreases below the holding point, the UJT turns "OFF" and as a result no current flows into the Emitter junction. Once again the capacitor charges up through resistor R_3 and this charging and discharging process between V_{ON} and V_{OFF} is constantly repeated while there is a supply voltage, Vs.

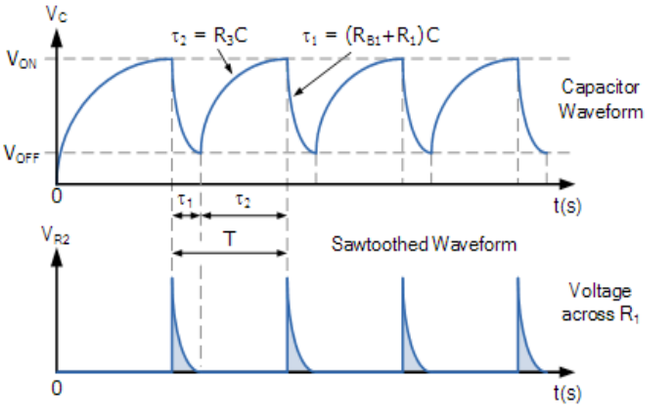

Fig. 2: *Voltage Across R_1*

UJT Relaxation Oscillation Waveform

It can be seen that the unijunction oscillator switches "ON" and "OFF" continually without any feedback. The operational frequency of the oscillator is directly affected by the value of resistor R_3, which has been used for charging in series with the capacitor C_1. The shape of the output pulse generated from the Base (B_1) terminal is that of a saw-tooth wave and to regulate its time period, only the ohmic value of resistance R_3 need to be changed since it sets the RC time constant for the capacitor.

The time period, T of the saw-tooth waveform can be determined as the charging time plus the discharging time of the capacitor. As the discharge time (τ_1) is generally very small in comparison to the charging time (τ_2) the time period of oscillation is equivalent to $T \cong \tau_2$. The frequency of oscillation is therefore given by $f = 1/T$. This can be understood by an example. Let a UJT, which gives the intrinsic stand-off ratio **η** as 0.65. If a 100nF capacitor is used, then calculate the resistor required to produce an oscillation frequency of 100Hz.

1. The timing period is given as:

$$f = \frac{1}{T}, \quad \therefore T = \frac{1}{f} = \frac{1}{100} = 10\text{mS}$$

2. The value of the timing resistor, R_3 is calculated as:

$$T = R_3 C \ln\left(\frac{1}{1-\eta}\right)$$

$$\therefore R_3 = \frac{T}{C \times \ln\left(\frac{1}{1-\eta}\right)} = \frac{10\text{mS}}{100\text{nF} \times \ln\left(\frac{1}{1-0.65}\right)}$$

$$\therefore R_3 = 95.238\Omega \text{ or } 95.3\text{k}\Omega$$

Then the value of charging resistor required in this example is 95.3kΩ's to the nearest preferred value. However, there are other conditions required for the UJT relaxation oscillator to operate correctly as the resistive value of R_3 can be extremely large or small.

In case if the value of R_3 is too large, in Megohms, the capacitor may not charge up sufficiently to trigger the Unijunction's Emitter into conduction. Likewise if the value of R_3 is too small, a few hundred Ohms, once triggered the current flowing into the Emitter terminal may be sufficiently large to drive the device into its saturation region preventing it from turning "OFF" completely. Either way the unijunction oscillator circuit would fail as an oscillator.

Experiment: To construct a UJT relaxation oscillator and plot the wave forms at emitter, Base1 and Base2.

Apparatus Required: Resistors 100 Ω (2), 10 KΩ (1), Capacitor 0.1 μF (1), UJT (1), Power supply 10 V DC (1), Oscilloscope 0 to 20 MHz (1), Multimeter (1), Bread Board (1), Connecting wires.

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Procedure

1. Assemble the circuit on a bread board as given in the Figure 3.

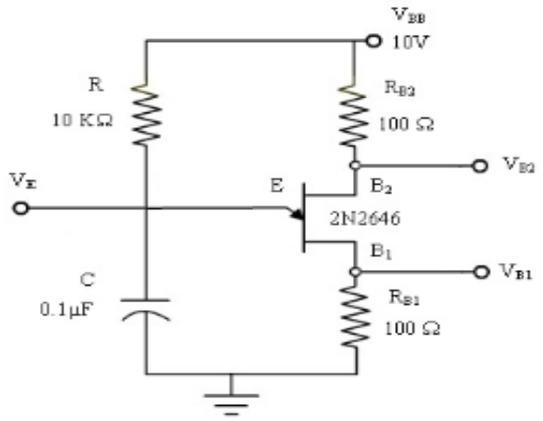

Fig. 3: *Circuit*

2. Connect the output of the circuit to an oscilloscope.
3. Switch ON the power supply and observe the wave forms at V_E,V_{B1},V_{B2}.
4. Measure the amplitude and time period of the wave forms.
5. Plot the expected waveform.

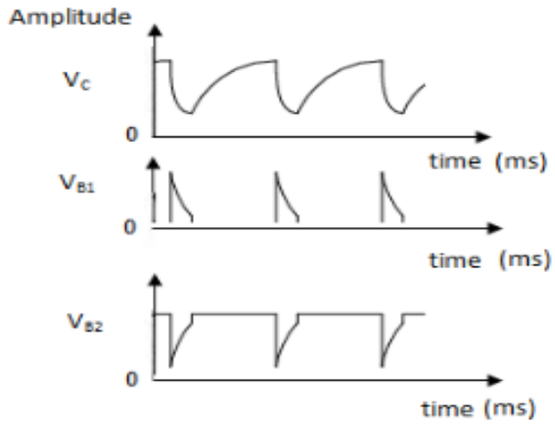

Fig. 4: *Expected Waveforms*

Precautions

1. The value of resistance R_3 much be in an appropriate range.
2. Make sure that all the connections established as given in the diagram are connected properly.

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8. ASTABLE MULTIVIBRATOR

Introduction

'Astable Multivibrator' is a switching circuit having two stage, in which the output of the first stage is fed to the input of the second stage and vice versa. Both of the stages gives a complementary output. This generates a square wave with no any external triggering pulse. The circuit has two switching states changing from one to another with time by discharging of a capacitor through a resistor.

Astable multivibrator also known as '**Free-Running Multivibrator'** as it does not require any additional inputs to oscillate. Astable oscillators produce a continuous square wave from its output because it have the pair of two cross-coupled transistor (Either n-p-n or p-n-p) with grounded emitter in its circuit. Both of the transistors are biased for linear operation and they operates as a Common Emitter Amplifiers having 100% positive feedback.

This configuration satisfies the condition for oscillation when one stage is switched "fully-OFF" (cut-off) while the other stage conducting "fully-ON" (Saturation). This gives a very high level of mutual amplification between the two transistors. By the capacitor discharging through a resistor, conduction is transferred from one stage to the other.

These are mostly used as relaxation oscillator because they are reliable, simple and ease of construction.

Theory

An astable multivibrator can be constructed using transistors or using 555 timer IC. Here we are discussing both in this theory section. Using 555 timer IC, in astable mode of operation, until the voltage across the capacitor reaches the threshold level of (2/3)*Vcc,* the timing capacitor charges up toward *Vcc* through *(RA + RB)* assuming that *VO* is *high,* initially. At this point comparator C_1 switches states, causing the flip-flop output *Q* to go *high*, i.e., *Q = V* (1). Thus the discharge transistor *Q1* is ON and then the timing capacitor C discharges through *RB* and *Q1* (pin 7 in Figure). Until the capacitance voltage drops to (1/3)*Vcc,* the discharging continues, at which point comparator C_2 switches states causing the flip-flop output *Q* to go *low,* i.e., *Q = V*(0), turning off the discharge transistor *Q1*. Now at this point the capacitor starts to charge again, as a result it works to complete the cycle.

The capacitor voltage and output voltage waveforms are shown in Figure 2. As shown here, the capacitor is periodically charged and discharged between (2/3) *Vcc* and (1/3)*Vcc,* respectively.

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$$Tc = (RA + RB)\ C\ In\ 2$$

$$= 0.693\ (RA + RB)\ C$$

The discharging time is given by,

$$T_D = R_B\, C\ In\ 2$$

$$= 0.639\ R_B\, C$$

The total period $T = T_C + T_D$

$$T = 0.693\ (R_A + 2R_B)\ C$$

And the frequency of oscillations will be

$$fo = \frac{1}{T} = \frac{1}{0.693(R_A + 2R_B)C}$$

$$fo = \frac{1.44}{(R_A + 2R_B)C}$$

The charging time is given by,

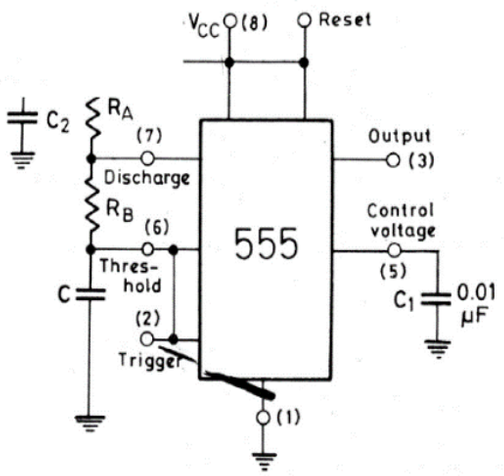

Fig. 1: *Circuit Diagram for A-stable Multivibrator*

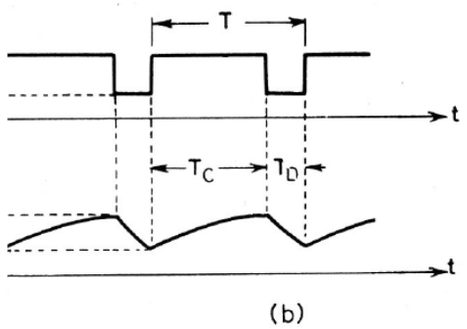

Fig. 2: *Capacitor and Output Voltage Waveforms*

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A-stable Multivibrator Using Transistor

The astable multivibrator circuit can be made up with two switching transistors, a cross-coupled feedback network, and two time delay capacitors. The delay capacitor allows multivibrator circuit to oscillate between the two states with no external triggering.

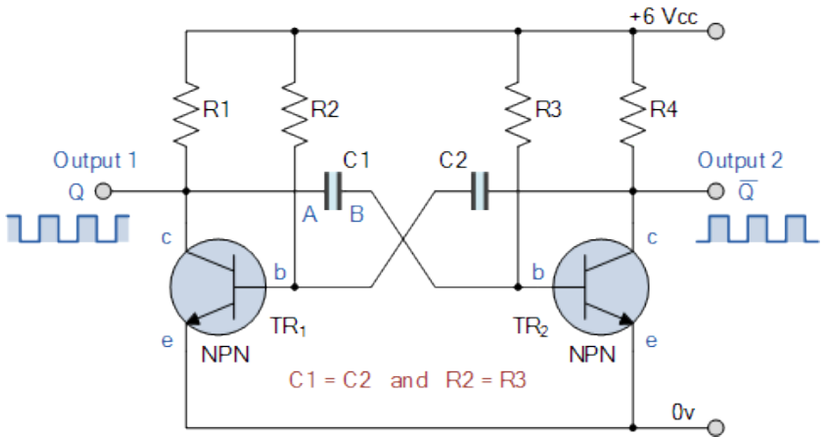

Fig. 3: *Circuit Diagram*

In the circuit shown in Figure 3, assume that transistor TR_1 is switched "OFF" (cut-off) and its collector voltage is increasing towards Vcc, while the other transistor TR_2 is turned "ON". Plate A of capacitor C_1 is connected to the collector of TR_1 which is now cut-off, so this rising towards the +6 volts supply rail of Vcc. There is no volt drop across load resistor R_1 since TR_1 is in cut-off.

Plate "B" on the other side of capacitor C1, is connected to the base terminal of transistor TR_2 and with 0.6V because transistor TR_2 is conducting (saturation). So there is a potential difference of +5.4 volts in the capacitor C_1 across its plates, (6.0 – 0.6v) from A to B.

The capacitor C_2 starts to charge up through resistor R_2 towards Vcc when the transistor TR_2 is ON. When the voltage across capacitor C_2 rises to more than 0.6v, it biases transistor TR_1 into conduction and turn it into saturation.

At any instant when transistor TR_1 switches "ON", plate "A" of the capacitor which was at Vcc potential, rapidly falls to 0.6 volts. This causes an equal and instantaneous fall in voltage on plate B. Therefore plate B of C_1 decreased to -5.4V. This negative voltage is then applied to the base of TR_2 which turn it OFF and lead it to the 'first unstable state'.

Now as the transistor TR_2 is into cut-off, so the capacitor C_1 is now begins to charge in the opposite direction via resistor R_3, which is also connected to the +6 volts V_{cc} supply. Thus the base voltage of transistor TR_2 is

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increasing in a positive direction with a time constant equal to the (C_1 x R_3) combination

However, transistor TR_2 never reaches at the value of V_{cc}, because when it get +0.6V, it turns fully "ON" into saturation. This action starts the whole process over again but this time with capacitor C_2 which is charging up via the resistor R2, took the base voltage of transistor TR_1 upto -5.4V and put it into the second unstable state.

We see that this circuit is alternating between one unstable state in which transistor TR_1 is OFF and transistor TR_2 is ON, and a second unstable in which TR_1 is ON and TR_2 is OFF. The rate of changing of states is determined by the RC values. As long as the supply voltage is present, this process will repeat itself over and over again.

The amplitude of the wave on output is approximately same as the supply voltage, Vcc. The time period of each changing state is determined by the time constant of the RC-networks which are connected to the transistor's base terminals. When the transistors are over-changing their-self in both "ON" and "OFF" states, the output at either collector will be a square wave with slightly rounded corners because of the current which charges the capacitors. This can be corrected by using more components in circuit.

When the two time-constants in the base circuits are same, then the output waveform will symmetrical in shape. By varying the capacitance of C_1, C_2 or the resistance R_2, R_3 the frequency of output wave can be altered.

Circuit Diagram

In the above figure of 555 Oscillator, the pin 6 and pin 2 are connected together. This allow the circuit to retrigger itself on each and every cycle. Also this allow it to operate as a free running oscillator. The capacitor C charges up by the both timing resistors, R_1 and R_2 during each cycle, but it discharges itself only through resistor R_2 because the other side of R_2 is connected with the discharge terminal which is on pin 7. Then the capacitor charges up to 2/3Vcc (the upper comparator limit) which is determined by the $0.693(R_1+R_2)C$ combination and discharges itself down to (1/3) Vcc (the lower comparator limit) determined by the 0.693(R2.C) combination. This now gives an output waveform of voltage level approximately equal to -1.5Volts V_{cc} and the outputs for "ON" and "OFF" time periods are determined using the capacitor and resistors combinations. Thus the individual time required to complete one charge and discharge cycle on the output is therefore calculated by:

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$T_1 = 0.693\ (R_1 + R_2)C,$

$T_2 = 0.693\ R_2\ C,$

$T = T_1 + T_2$

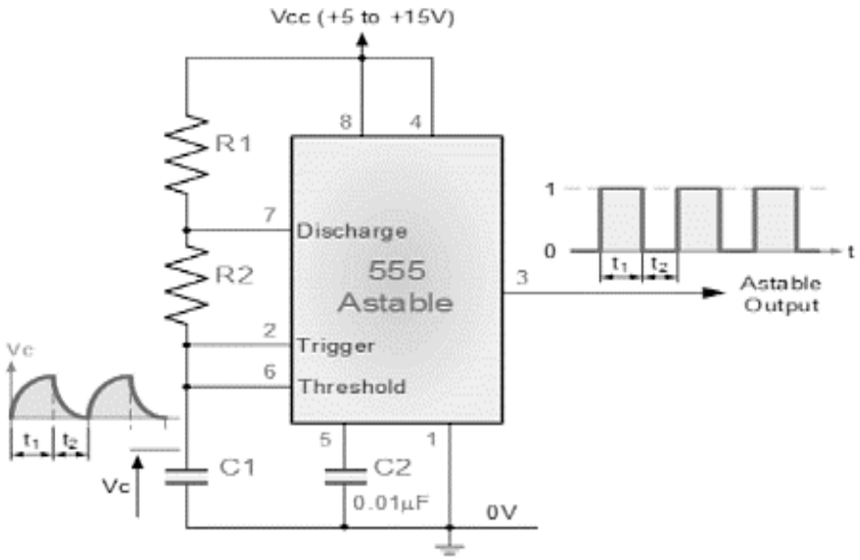

Fig. 4: *Circuit Diagram for A-stable Multivibrator*

Experiment: To design and test performance of an Astable Multivibrator to generate clock-pulse for a given frequency.

Apparatus Required: For Transistor based multivibrator Resistors 3.3KΩ-2, 10KΩ-2, Capacitors 0.1 µf - 2, Transistors 2N2369 – 2, Function Generator, CRO, Bread Board, Connecting Wires and Probes.

For 555 timer IC based multivibrator - 555 IC Timer, Resistor 10 KΩ-1, Capacitors 10nF, 0.1µF, 0.01µF, Function Generator, CRO, Bread Board, Connecting Wires and Probes.

Procedure

1. Connect the circuit on the bread board using the mentioned diagram.
2. Connect the CRO with the input and output terminals and spot the waveforms.
3. Trace these waveforms and find out its frequency.

Observation

Trace the output waveform from CRO and calculate the frequency after calculating the fundamental period of the wave.

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9. MONOSTABLE MULTIVIBRATOR

Theory

A monostable multivibrator has only one established state, the other state being quasi-stable. Commonly the multivibrator is in the stable state, but it switches from the stable to the quasi-stable state when an external triggering pulse is applied. It rests in the quasi-stable state from a short duration, but spontaneously reverts, i.e., shifts back to its original stable state, without any triggering pulse.

Operation Principle

In a monostable multivibrator, collectors are coupled of both transistors Q_1 and Q_2. Normally Q_1 is OFF and Q_2 is ON. Resistor R_1 and R_2 are connected to the transistor which is normally OFF, and the capacitor C is connected to the transistor which is ON.

It is comprehended from the circuit of the monostable multivibrator that, under standard circumstances, the supply voltage V_{CC} provides adequate base drive to the transistor Q_2 through resistor R, with the consequence that Q_2 goes into saturation.

With Q_2 ON, Q_1 goes OFF. When Q_2 is ON and Q_1 is OFF, then the capacitor catches a charging path. The voltage across the capacitor is V_{CC} with polarity. It is observable that in the stable state of the multivibrator, the transistor Q_2 is ON and Q_1 is OFF.

The collector of Q_1 transistor is transmitted to the base of Q_2 through the capacitor, If the negative triggering pulse is applied on it. This makes the base of transistor Q_2 negative. Instantly the transistor Q_2 goes OFF and Q_1 becomes ON. Still, this is only a quasi-stable state as it is apparent form the following observation.

When the transistor Q_1 is ON and transistor Q_2 is OFF, the capacitor C finds a discharging path for it. As the capacitor discharges, it is comprehended that the potential at the base of the transistor Q_2 turn out to be less and less negative, and after an stage, we have V_B = Vg, which is the cut-in-voltage of Q_2.

The transistor Q_2 starts conducting and gets saturated when the voltage V_B crosses the level of Vg, thus the transistor Q_2 becomes ON, and Q_1 becomes OFF. Thus the novel unwavering state of the multivibrator is re-established.

In quasi-stable state, Q_1 is ON and Q_2 is OFF.

The interval through which the quasi-stable state of the multivibrator continues, i.e., the transistor Q_2 remains OFF, is hooked on the rate at which

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the capacitor C discharges. This duration of the quasi-stable state is called 'delay time' or 'pulse width' or 'gate time' and it is represented by T.

Monostable Multivibrator Using 555 Timer IC

It contains one stable and one quasi stable state. To response a triggering signal, for generating single output pulse of time duration, the circuit is useful. The external components connected to the op-amp are very useful to the width of the output pulse. A negative triggering pulse is given by the diode.A diode clamps the capacitor voltage to 0.7V when the output is +Vsat, then a negative going triggering pulse of magnitude V_i passed through the RC and other there a negative triggering pulse is applied to the positive terminal (Refer Figure 1).

The values of the resistance R and the capacitor C,which are external to chip, determine the output pulse width. The voltage at the trigger input pin is *high* before the application of the trigger pulse *vt* ,which is equal to *Vcc* [say *V*(1)]. With this high trigger input, the flip-flop output *Q* to be *high*, i.e., *Q* = *V*(1) and *Vo* = *V* (0) = 0 (due to inverter circuit),since the output of comparator C_2 is *low* [say *V*(0)],. The discharge transistor *Q1* will be saturated with *Q* = *V* (1) and the voltage across the timing capacitor C will be essentially zero, that is, *Vx* = O. The quiescent state of the timer device is output *Va* = 0 V. At *t* = 0, the application of trigger v_t less than *Vcc/3* causes the output of comparator C_2 to be *high*, i.e., *V* (1). This will set the flip-flop with *Q* = *low.*, i.e., *Q* = *V* (0). This makes *Vo* = *V* (1). The transistor will be turned 'OFF' due to *Q* = *V*(0) discharge. Note that the flip-flop will remain in the *Q* = *V*(0) state after termination of the trigger pulse.

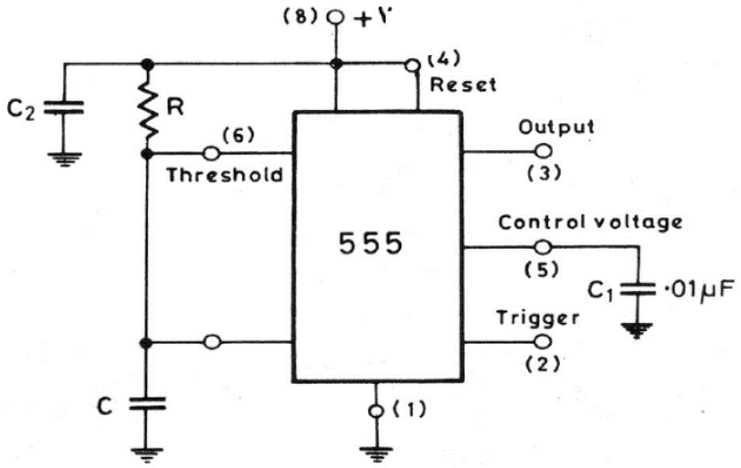

Fig. 1: *Monostable Multivibrator using 555 Timer IC*

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Figure 2 Illustrates the circuit diagram for monostable multivibrator.

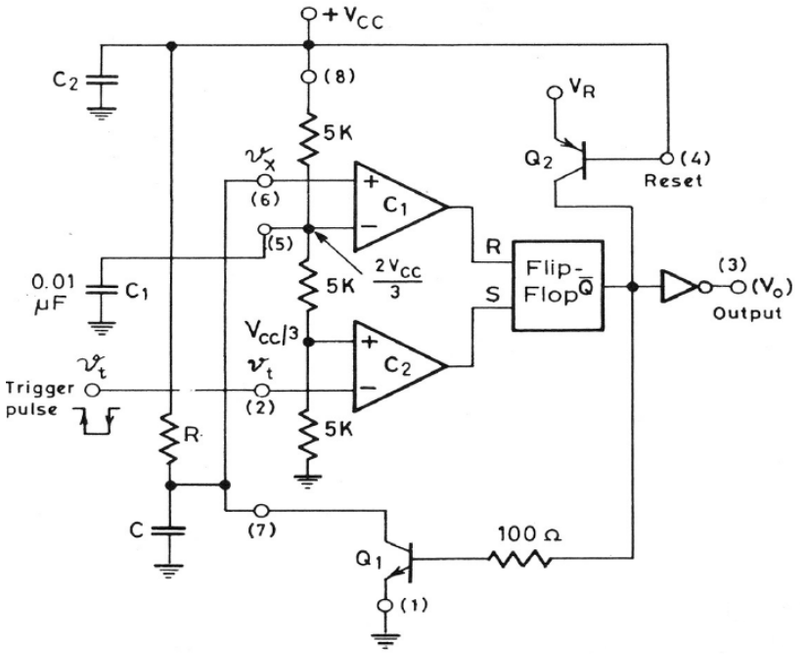

Fig. 2: *Circuit Diagram*

Now, with a time constant $t = RC$, the timing capacitor charges up toward *Vcc* through resistor *R*. The charging up expression is

$$V_x = V_{CC}\,(1 - e^{-t/RC}) \qquad ...(1)$$

where v_x is voltage across C at a time *t*.

Comparator C_1 will switch states and its output voltage will now be *high,* when v_x reaches the threshold voltage level of $2Vcc/3$,. This causes the flip-flop to reset as result *Q* will go *high*, i.e., $V(1)$, and V_0 come in their original level $V(0)$. The discharge transistor *Q1* turns on because of the high value of *Q*. The capacitor C discharges quickly as a reason of low saturation resistance of *Q1*. the output pulse turn to end at time T1, at which point $v_x = 2\ (1/3)V_{CC}$. Thus the pulse width T1 is calculated by the time required for the capacitor voltage v_x to charge from zero to $2V_{CC}/3$. This period can be calculated by putting $v_x = (2/3)V_{CC}$ at $t = T$, Thus from Equation 1,

$$2\,V_{CC}/3 = V_{CC}\,(1 - e^{-T_1/RC})$$

$$T_1 = RC \ln \frac{V_{CC}}{V_{CC} - \frac{2}{3} V_{CC}}$$

$$T_1 \cong 1.1\,RC \qquad ...(2)$$

Here it is noted that the pulse duration does not depend upon the supply voltage *Vcc.* For proper operation of the timer, the trigger pulse width must be shorter in duration than T1. In Equation 2 we have assumed $V(0) = 0$. By connecting the reset terminal (pin 4), the timing cycle may be interrupted. Thus the transistor *Q1* turned ON and the capacitor is now prevented from charging.

In case of 555 timer IC the values of the resistance R and the capacitor C,which are external to chip, determine the output pulse width. The voltage at the trigger input pin is *high* before the application of the trigger pulse *vt* ,which is equal to *Vcc* [say $V(1)$]. With this high trigger input, the flip-flop output *Q* to be *high*, i.e., $Q = V(1)$ and $Vo = V(0) = 0$ (due to inverter circuit),since the output of comparator C_2 is *low* [say $V(0)$].

The discharge transistor *Q1* will be saturated with $Q = V(1)$ and the voltage across the timing capacitor C will be essentially zero, i.e., $Vx = O$. The quiescent state of the timer device is output $Va = 0$ V. At $t = 0$, the application of trigger v_t, (negative going pulse shown in [Fig.*(b)*] less than *Vcc/3* causes the output of comparator C_2 to be *high*, i.e., $V(1)$. This will set the flip-flop with $Q = low$. i.e., $Q = V(0)$. This makes $Vo = V(1)$. The transistor will be turned 'OFF' due to $Q = V(0)$ discharge. Note that the flip-flop will remain in the $Q = V(0)$ state after termination of the trigger pulse. Now, with a time constant $t = RC$, the timing capacitor charges up toward *Vcc* via resistor *R.* The charging up expression is,

$$V_x = V_{CC}(1 - e^{-t/RC}) \qquad ...(3)$$

where v_x is voltage across C at a time *t.*

Experiment: To design and check the performance of a monostable multivibrator which generate clock pulse for a given frequency and get the waveforms.

Apparatus Required: For transistor based monostable multivibrator -Resistors 2.2KΩ-2, 10KΩ-1, 1KΩ-2, 1.5 KΩ-1, Capacitors- 0.1μF, 1 μF, Transistors 2N2369 – 2, Diode QA79-1, CRO, Power supply 0-30V, Bread board, Connecting wires.

For 555 timer IC - 555 IC Timer, Resistor10 KΩ, Capacitors 10nF, 0.1μF, 0.01μF, Function Generator, CRO, Bread Board, Connecting Wires and Probes.

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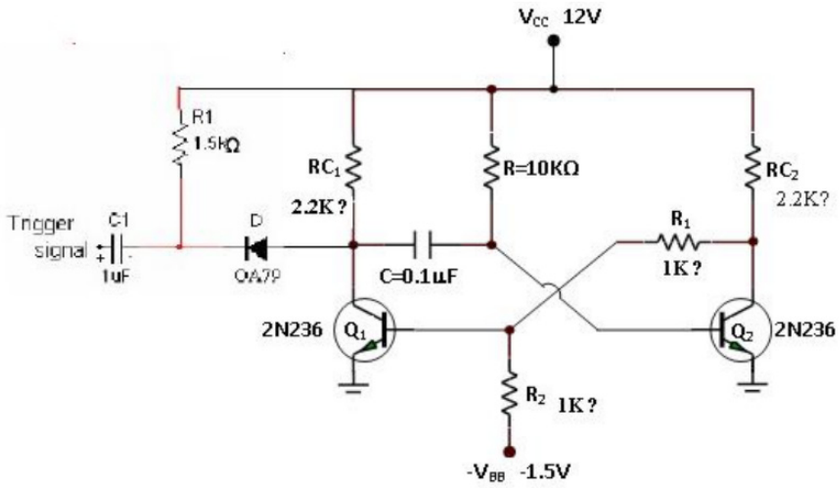

Fig. 3. *Monostable Multivibrator: Circuit Diagram*

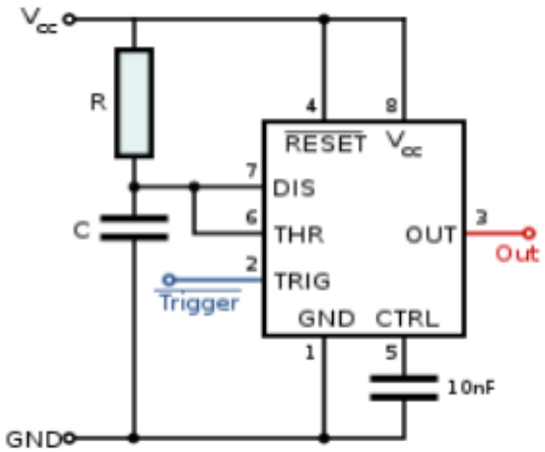

Fig. 4: *RESET State*

Procedure

1. Connect the whole circuit as shown in the circuit diagram of Figure 3.
2. Now apply negative triggering pulses of frequency 1 KHz at pin 2, as shown in Figure 4.
3. Observe the capacitor voltage and trace the output waveform from CRO (as shown in Figure) and than measure the pulse duration.
4. Now use the theoretical expression and calculate the pulse duration like T_{high} =1.1 RC
5. Compare the theoretical values with experimental values.

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10. TRANSISTORIZED HARTELY AND COLPITTS AUDIO OSCILLATOR

Introduction

Hartley oscillator was invented in 1915 by Ralph Hartley when he was working for the Western Electric Company. The original design was based on a tube based. In a Hartley oscillator, the oscillation frequency is established by a tank circuit consisting of two inductors and one capacitor. The inductors were connected in series and the capacitor was connected across parallel. Hartley oscillators are generally used in Radio Frequency (RF) oscillator applications and the proposed frequency range is from 20KHz to 30MHz. Hartley oscillators can be used at frequencies lower than 20KHz, however for lower frequencies, the inductor value require to be high and it has a practical limit.

Theory

The circuit diagram of a typical Hartley oscillator is shown in the Figure 1 below.

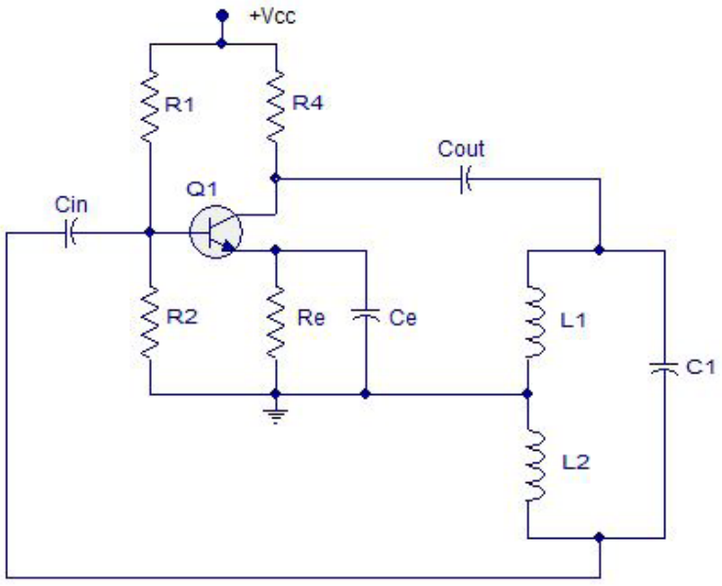

Fig. 1: *Hartley Oscillator*

In the circuit diagram resistors R_1 and R_2 offer a potential divider bias for the transistor Q_1. R_E is the emitter resistor, its job is to give thermal stability for the transistor. C_E is the emitter by-pass capacitors, that by-passes the improved AC signals. If the emitter by-pass capacitor is not present, the

amplified AC voltages will go down across R_E and it will be added on to the base-emitter voltage of Q_1 and will interrupt the biasing conditions. C_{IN} is the input DC decoupling capacitor whilst C_{OUT} is the output DC decoupling capacitor. The work of a DC decoupling capacitor is to avoid DC voltages from achieving the succeeding stage. Inductor L_1, L_2 and capacitor C_1 structures the tank circuit.

When the power supply is switched ON the transistor begins conducting and the collector current increases. Consequently the capcitor C_1 starts charging and when the capacitor C_1 is fully charged it begins to discharge through coil L_1. This charging and discharging generates a series of damped oscillations in the tank circuit.

The oscillations generated in the tank circuit is coupled to the base of Q_1 and it emerges in the amplified appearance across the collector and emitter of the transistor. The output voltage of the transistor (voltage across collector and emitter) should be in phase with the voltage across inductor L_1. As the junction of two inductors is grounded, the voltage across L_2 will be 180° out of phase to the voltage across L_1. The voltage across L_2 is in fact fed back to the base of Q_1. From the above discussion, the feed back voltage is 180° out of phase with the transistor and as well the transistor would create another 180° phase difference. Thus the total phase difference between input and output is 360° and it is imperative provision for creating sustained oscillations.

Working

When the supply is switched–ON, a voltage V_1 is built up across L_1 and V_2 across L_2. V_1 is referred to as the oscillator output. There is a phase difference of 180^o in the voltage of L_1 and L_2. The voltage across L_2 (V_2) is referred as the feedback signal. As the amplifier is in CE arrangement, it generates a phase difference of 180^o. Hence, amplifier and the feedback network generates a phase difference of 360^o, .i.e, a positive feedback is accomplished and circuit works as an oscillator.

When energy is supplied to the tank circuit, cycle starts. The capacitor accumulates energy in its electric field every time there is a potential difference across its plates. As the current starts to run out of the capacitor and into the inductor, a magnetic field builds up around the coil. Capacitor loses its energy and current will continue to flow in the inductor due to the effect of the energy in the magnetic field. This current starts to send current back into the capacitor, in reverse direction. The cycle then recurs, again and

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again, at a period (frequency) that is established by the values of the inductor, the capacitor. The frequency of oscillation is given by,

$$f = \frac{1}{2\pi\sqrt{LC}}$$

Experiment: To design and construct a Hartley and Colpitts oscillator and to measure its output frequency.

Apparatus Required: Transistor - BC107 - 1, Capacitors- 0.1μF, 10μF - 1 each and 0.22 μF - 2, Resistors - 47kohm, 1kohm and 10kohm - 1 each, Decade inductance box (DIB) - 1**,** Decade Resistance Box (DRB) - 1, Inductors : 5mH – 2, CRO(Dual Channel) - (0-20 MHz), Function generator - (1Hz to 1 MHz), Regulated power supply - (0-30V), Bread Board, Connecting wires.

Procedure

1. Connections are to be made according to the circuit diagram carefully and properly (C_1 value to be selected as 0.1μF and 10μF as required).
2. Connect CRO at output terminals and monitor the wave form.
3. Calculate experimentally the frequency of oscillations by using the expression.

   $f = 1/T$, Where T = Time period of the waveform
4. Repeat the procedure for various values of L_1 and note down experimental values of oscillations of Hartley oscillator.
5. Evaluate the values of frequency of oscillations both theoretically and experimentally.

Precautions

1. All the connections are to be made carefully and properly.
2. Transistor terminals must be identified appropriately.
3. Readings should be noted avoiding any parallax error.

Colpitts Oscillator

Theory

The tank circuit is constructed of L_1, C_1 and C_2 .The resistance R_2 and R_3 gives the necessary biasing. The capacitance C_3 blocks the DC component. The frequency of oscillations is choosen by the values of L_1,C_4 and C_5, and is specified by,

$$f = \frac{1}{2\pi(C_T L_1)^{1/2}}$$

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Where $C_T = C_1C_2 / (C_1 + C_2)$

The energy delivered to the tank circuit is of in phase. The tank circuit provides 180° out of phase. Additionally, the transistor offers another 180°. This way, energy feedback to the tank circuit is in phase with the fabricated oscillations.

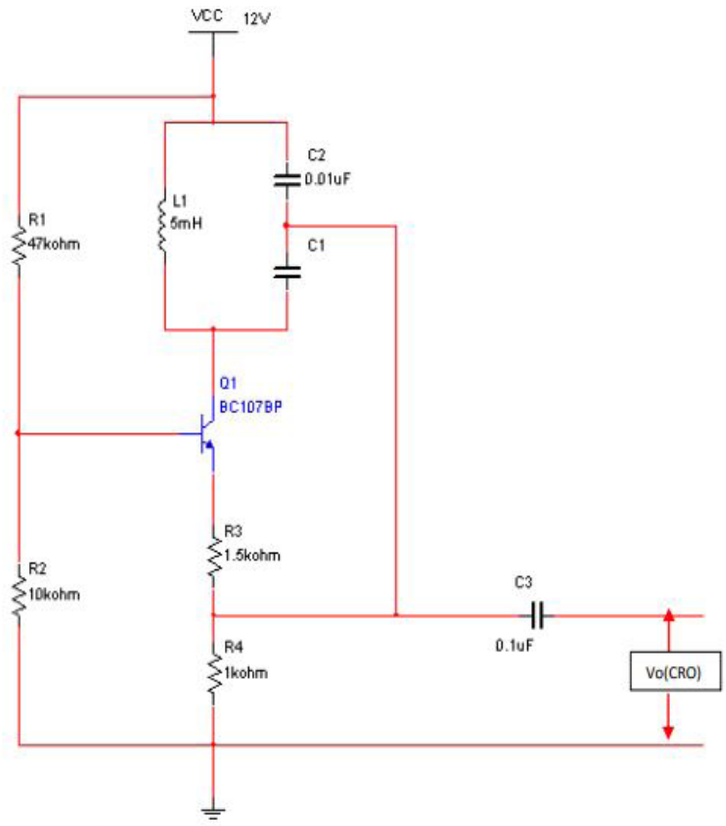

Fig. 2: *Colpitts Oscillator*

Colpitts Oscillator Circuit

All oscillator circuits that creates sinusoidal waveforms make use of the LC resonant circuit apart from a few electronic circuits such as RC oscillators, Wien-Robinson oscillator and a few crystal oscillators that do not need extra inductances for this reason.

It can be realized by means of gain device for instance Bipolar Junction Transistor (BJT), operational amplifier and Field Effect Transistor(FET) as comparable in other LC oscillators also. The capacitors C_1 and C_2 forms potential divider and this tapped capacitance in the tank circuit can be utilized as the source for feedback and this setup can be employed to supply

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better frequency stability in contrast to the Hartley oscillator where tapped inductance is used for feedback setup.

R_E resistor in the circuit provides balance for circuit against discrepancy in temperature. The capacitor C_E connected in the circuit is parallel to the R_E, gives low reactive path to the amplified AC signal performing as Bypass capacitor. The Resistors R_1 and R_2 form voltage divider for circuit and offer bias to the transistor. The circuit posses of a RC coupled amplifier with common emitter configuration transistor. The coupling capacitor C_{OUT} obstructs DC by providing an AC path from the collector to the tank circuit.

Working

Every time power supply is switched on, the capacitors C_1 and C_2 begin charging and after the capacitors get fully charged, the capacitors begin to discharge from the inductor L_1 in the circuit inducing damped harmonic oscillations in the tank circuit.

Consequently, an AC voltage is generated across C_1 and C_2 by the oscillatory current in the tank circuit. Whereas these capacitors get fully discharged, the electrostatic energy stored in the capacitors gets carried in the form of magnetic flux to the inductor and so inductor gets charged. Correspondingly, when the inductor starts discharging, the capacitors begins to charge again and this procedure of energy charging and discharging capacitors and inductor continues producing the generation of oscillations and the frequency of these oscillations can be verified by using the resonant frequency of the tank circuit comprising of inductor and capacitors. This tank circuit is believed as the energy reservoir or energy storage. This is due to the frequent energy charging and discharging of the inductor, capacitors that are a component of LC network forming the tank circuit.

The incessant undamped oscillations can be attained from the Barkhausen criterion. For sustained oscillations, the total phase shift must be 360^o or 0^o. In the given circuit as two capacitors C_1 and C_2 are center tapped and grounded, the voltage across capacitor C_2 (feedback voltage) is 180^o with the voltage across capacitor C_1 (output voltage). The common emitter transistor gives 180^o phase shift among the input and output voltage. Therefore, from the Barkhausen criterion we can get undamped continuous oscillations.

The resonant frequency is given by,

$$f = \frac{1}{2\pi\sqrt{(CL_1 + C)}}$$

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Where f_r is the resonant frequency, C is the equivalent capacitance of series combination of C_1 and C_2 of the tank circuit and L_1 represents the self inductance of the coil.

Here C is given as,

$$C = (C_1 \times C_2) / ((C_1 + C_2))$$

AIM: To study and calculate frequency of oscillations of Colpitts oscillator.

Apparatus Required: Transistor BC 107 - 1, Capacitors 0.1μF - 1 and 0.01μF - 2, Inductor 5mH - 1 Resistors 47kohm, 1kΩ, 10kΩ, 1.5K - 1, Decade inductance box, CRO(Dual Channel) (0-20 MHz), Function generator (1Hz to 1 MHz), Regulated power supply (0-30V), Connecting wires.

Procedure

1. Connections are to be complete according to the circuit diagram.
2. Attach CRO output terminals and examine the waveform.
3. Calculate experimentally the frequency of oscillations from the expression

   $f = 1 / T$ (where, T = Time period of the waveform).
4. Follow and repeat the procedure in the the above steps 2,3 for various values of L, and record the experimental values of oscillations of the Colpitts oscillator.

Precautions

1. The connections are to be connected carefully and appropriately.
2. Transistor terminals should be identified correctly.
3. Readings should be recorded without any parallax error.
4. Evaluate the values of oscillations both theoretically and experimentally.

11. MICHELSON'S INTERFEROMETER

Introduction

The Michelson interferometer is being used for the observation of interference phenomena; for example - interference at equal inclination, interference at equal thickness, interference of white light, getting precise wavelength contrast, determination of zero path difference and for measuring the refractive index of a transparent medium or air.

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Theory

Interference: Light is an electromagnetic wave comprising two vectors: one of which is an electric field vector and another one is a magnetic field vector. These two vectors collectively can model a light waves. When two or more beams of light interfere with each other in the space, these field vectors add up constructively or destructively according to the well known phenomenon of principle of superposition. These light beams are independent of each other hence they have no fixed relationship. At any time in space there will be points where the field vectors add up constructively to produce the maximum field strength. Similarly at some other instant that point in space may have a minimum field strength. The oscillations of the visible light are faster than the perceiving power of human eye. The human eye averages out these intensities and ultimately perceives a uniform intensity of light.

In other case, if the light beams come from the same coherent source, then there will always be a relationship between the frequency and phase of the beams. At any point in space the light from the beams will always be in a specific phase difference. So the combination of these two will always be of same intensity. There will be a bright spot in case of constructive add up and a dark spot in case of a destructive add up. This phenomenon is called as interference.

In year 1801, Scientist Thomas Young designed a method to produce an interference pattern. He just allowed a single and narrow beam of light to fall upon two narrow and close slits of light. A screen was placed opposite to the slits. When the light coming out of these two slits overlaps on the screen, a regular pattern of alternate dark and bright bands appear.

Young's experiment opened out important evidences to explore the wave nature of light. A set of two slits can be used as a simple interferometer. If the distance between the slits is known, the width of the maxima and minima pattern observed on the screen can be used to determine the wavelength of the light. Alternatively, if the wavelength of the light is known, the distance between the slits could be determined from the width of dark and bright patterns of interference.

Michelson Interferometer: Michelson designed and constructed an interferometer based on interference principle. In fact the interferometer was designed as a means to test the existence of ether, which is a hypothetical medium through which the light can propagate. This hypothesis was discarded as the results of this experiments came to be against this thesis. So, now it is no longer considered a viable hypothesis. However, Michelson's interferometer

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has now become a widely used instrument for the measurement of the wavelength of light. This is also used for measuring very small distances by using any source of identified wavelength, and for investigating the refractive index of an optical media.

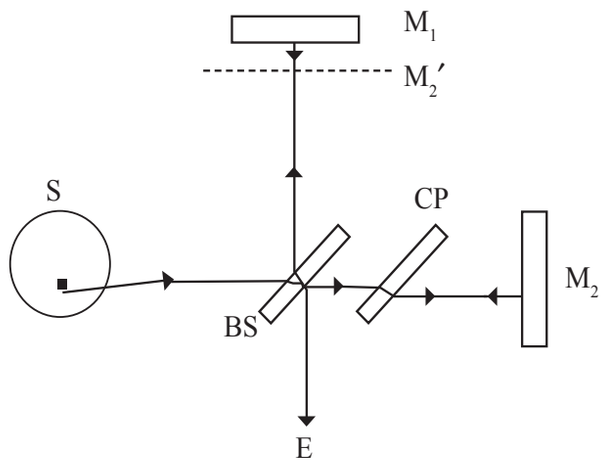

Fig. 1: *Michelson Interferometer*

Figure 1 shows a diagram of Michelson's Interferometer. Firstly, the beam of light from the Source (S) strikes the beam splitter, this splitter reflects 50% of the light falling on it and transmits the other 50% of it. The incident beam splits into two beams; one beam is reflected toward the mirror M_1, which is fix at its place. The other beam is transmitted toward the movable mirror M_2. Then both of these mirrors reflect the light back toward the Beam Splitter (BS). The light reflected from mirror M_1 is transmitted through the Beam splitter (BS) to the detector E, and the other light reflected form M_2 is first transmitted through the plate CP and then reflected by the beam splitter (BS) to the detector E. These rays interfere with each other and give an interference pattern.

In Figure 1, M_2' is a virtual image of the mirror M_2. The path of light in the Michelson interferometer can be seen as the path of light in the air plate present between M_1 and M_2'.

The Compensator Plate (CP) which is parallel to the Beam Splitter (BS) has the same thickness and refractive index as of beam splitter. Because the paths of light of the two beams should be equal, and different light beams should have the same retardation. It is also very easy to observe the white light interference. The process of the formation of the interference rings is shown in Figure 2.

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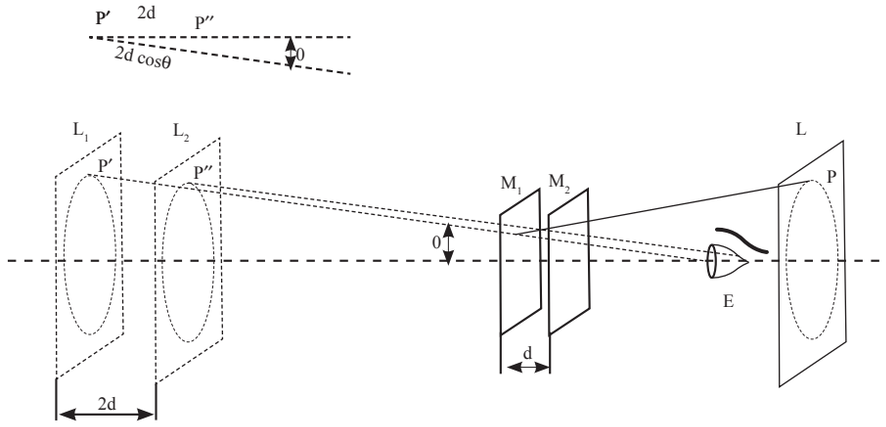

Fig. 2: *Formation of Interference Rings*

As we have discussed that M_2' is the virtual image of mirror M_2, it is also parallel to the mirror M_1. For an ease, let us consider that the light source L is at the observer's position. L_1 and L_2 are the virtual images of source L formed by the mirrors M_1 and M_2'. Let us consider that d is the distance between M_1 and M_2, hence the distance between light sources L_1 and L_2 is $2d$. So, if $2d = \lambda n$; (n is an integer), evidently the phases of the light coming from the normal direction of the sources L_1 and L_2 are the same, but the phase of the beam coming from the other directions is not same. Light beams coming from the points P′ and P″ have a path difference of $2d\ cos\theta$. In case, if M_1 is parallel to M_2, the two light beams are parallel to each other. So, whenever $2d\ \cos\theta = n\lambda$ (where, n is an integer), the two light beams construct a maximum field strength. For definite values of n, λ and d, the value of θ is a constant. In this way the contour of the maximum intensity points altogether become a ring. At $\theta = 0$, the condition for a bright fringe becomes $2d = \lambda n$.

Experiment: To determine the wavelength of a sodium light using Michelson Interferometer.

Apparatus Required: A light source (Sodium Lamp), A lens, a telescope and Michelson Interferometer.

Procedure

1. Set the interferometer somewhere in the middle. In this position, the association between the interferometer reading and the mirror movement will be almost linear (Refer Figure 3).
2. Make a full turn of the interferometer screw before counting fringes. It is to eliminate errors occurred because of backlash. Always move the interferometer in one direction only.
3. Adjust the interferometer to produce the circular fringes.

4. At this position, you have a clear equal inclination fringes with bright fringe at the centre (that is θ = 0), observe the initial reading of the interferometer and name it as *d*1.
5. Now, measure the covered distance by the interferometer after each and every 20 fringes. Give them values such as x_1, x_2, x_3, ..., and so on. Calculate the actual distance moved by the interferometer for 100 fridges. Average them out to get least errors.

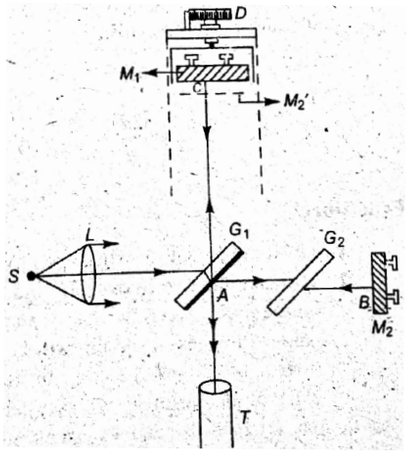

Fig 3: *Appratus Setup*

Use the following expression and calculate the wavelength of the sodium light.

$$\lambda = \frac{2d}{n}$$

If mirror M_1 is moved by the distance *d* then the shift in fringes is mentioned as *n*.

S. No.	No. of Fringes	Micrometer Reading	Distance Moved for 100 Fringes, *d*
1.	0	x_1	—
2.	20	x_2	
3.	40	x_3	
4.	60	x_4	
5.	80	x_5	
6.	100	x_6	$x_6 - x_1$
7.	120	x_7	$x_7 - x_2$
8.	140	x_8	$x_8 - x_3$
9.	160	x_9	$x_9 - x_4$
10.	180	x_{10}	$x_{10} - x_5$

Wavelength of the sodium light is - .....

Precautions

1. The telescope must be focused properly to observe sharp fringe edges.
2. Counting of fringes is a matter of concern as the answer majorly depends on that.

12. ULTRASONIC INTERFEROMETER

Introduction

Ultrasonic interferometer is a straightforward device that generates precise and consistent data, from which the velocity of ultrasonic sound in a liquid medium can be determined with a high degree of efficiency. A crystal controlled interferometer operating frequencies ranging from 1 to 12 MHz has been used to compute the ultrasonic velocity.

Theory

Ultrasonics

Ultrasonic sound indicates to a sound pressure with a frequency larger than the human range (20 Hz to 20 KHz). When an ultrasonic wave propagates via a medium, the molecules in that medium vibrate over small distance in a direction corresponding to the longitudinal wave. Through this vibration, momentum is transmitted between molecules. This causes the wave to pass from the medium.

Ultrasonic Interferometer

An ultrasonic interferometer is an uncomplicated and straight machine to establish the ultrasonic velocity in liquid with a high degree of precision.

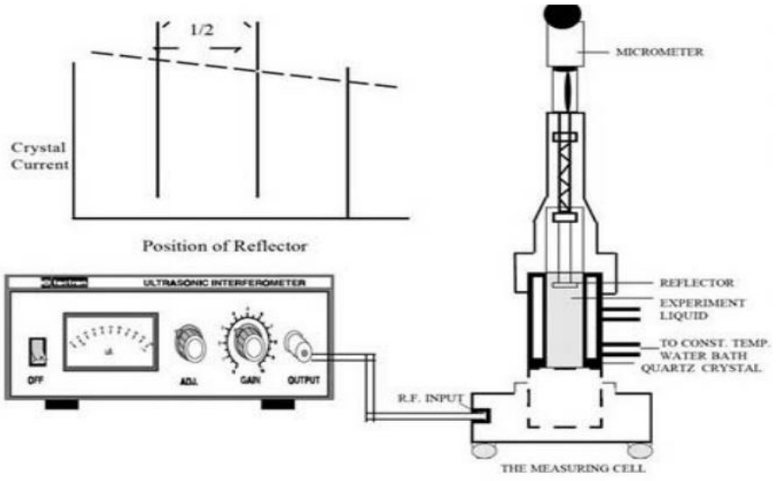

Fig. 1: *Ultrasonic Interferometer*

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Generation of Ultrasound

Ultrasonic waves can be generated by various methods. The most general methods consist of the following:

Mechanical Method*:* The ultrasonic frequencies up to 100 KHz are created. However, this technique is infrequently used owing to its limited frequency range.

Piezoelectric Methods : In ultrasonic interferometer, the ultrasonic waves are formed by the piezoelectric methods. At a fixed frequency changeable path interferometer, the wavelength of the sound in an experimental liquid medium is determined, and from this its velocity through that medium is computed. The ultrasonic cell is comprised of a double walled brass cell with chromium plated surfaces having a volume capability of 10 ml. The double wall permits water circulation around the experimental liquid to sustain it at a known constant temperature. The micrometer scale is marked in units of 0.01 mm and has on the whole length of 25 mm. Ultrasonic waves of identified frequency are generated by a quartz crystal that is preset at the bottom of the cell. There is a variable metallic plate parallel to the quartz plate, which reflects the waves. The waves impede with their reflections, and if the separation between the plates is accurately an integer multiple of half wave length of sound, standing waves are created in the liquid medium. Under these circumstances, acoustic resonance arises. The resonant waves are highest in amplitude, causes a analogous maximum in the anode current of the piezoelectric generator. The ultrasonic interferometer consists of the following mostly two parts:

(i) The High Frequency Generator

The high frequency generator is constructed to excite the quartz crystal set at the bottom of the measuring cell at its resonant frequency to produce ultrasonic waves in the experimental liquid filled in the "measuring cell". A micrometer to examine the changes in current two controls for the reason of sensitivity regulation and primary adjustment of the micrometer are supplied on the panel of the high frequency generator.

(ii) The Measuring Cell

The measuring cell is particularly designed for sustaining the temperature of the liquid steady throughout the experiment. A fine digital micrometer screw (LC 0.001 mm) has been offered at the top, that can lower or raise the reflector plate in the liquid inside the cell through a known distance. It has a quartz crystal set at its bottom.

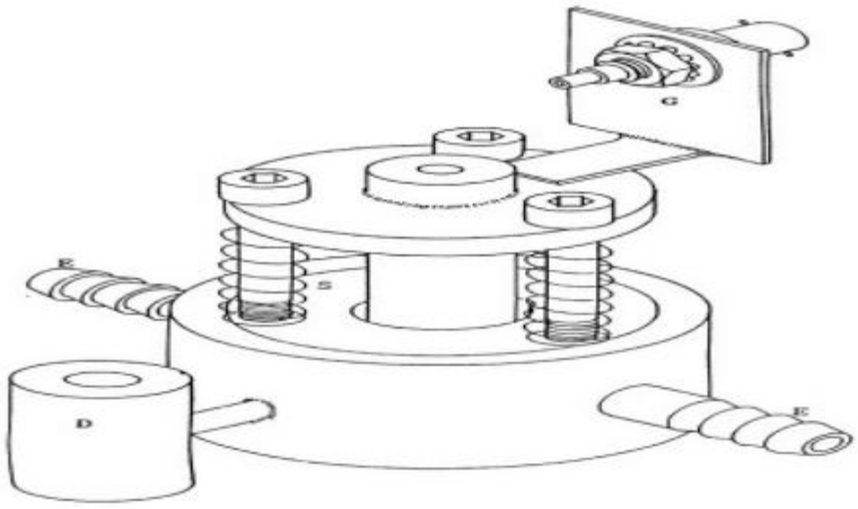

Fig. 2: *Schematic Diagram of Ultrasonic Interferometer*

Working Principle

The principle employed in the measurement of velocity (U) is based on the precise ascertain of the wavelength (λ) in the medium. Ultrasonic waves of known frequency (*f*) are generated by quartz crystal set at the bottom of the cell. These waves are reflected by a variable metallic plate set parallel to the quartz crystal. If the separation between these two plates is accurately a whole multiple of the sound wavelength, standing waves are created in the medium. This acoustic resonance produces an electrical reaction on the generator driving the quartz crystal and anode current of the generator develop into a maximum. If the distance is increased or decreased and the difference is exactly one half wavelengths (λ/2) or multiple of it, anode current happen to be maximum from the knowledge of wavelength (λ) the velocity (U) can be obtained by the relation:

$$\text{Velocity} = \text{Wavelength} \times \text{Frequency}$$

$$U = \lambda \times f \qquad \ldots(1)$$

Adjustment of Ultrasonic Interferometer

For primary adjustment two knobs are presented on high frequency generator, one is marked with "ADJ" to regulate the position of the needle on the ammeter and the knob marked "GAIN" is used to amplify the sensitivity of the instrument for greater deflection. The ammeter is used to observe the number of maximum deflection although micrometer is moved up or down in liquid.

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Measurement of the Density

The density measurements were completed by dilatometer. It was positioned in a high precision water bath for temperature control. The dilatometer was calibrated primarily by means of distilled water. The consistency of the dilatometer was checked for liquid like benzene and carbon tetrachloride at recognized temperatures. The densities measured for A.R. grade benzene and carbon tetrachloride were established to be 0.8735 and 1.5845 g/cc, respectively at 298.15K. The literature values of densities for benzene and carbon tetrachloride were estimated to be 0.8737 and 1.5844 g/cc, respectively. Consequently, the measured values were in good agreement with their literature values.

Experiment : To estimate the velocity of ultrasonic sound through different liquid media.

To estimate the adiabatic compressibility of the given liquid.

Apparatus Required: The Ultrasonic Interferometer, sample liquids, high frequency generator.

Procedure

1. Unscrew the cap of cell and lift it from double walled construction of the cell. In the middle position of it dispense experimental liquid and rotate the cap. Wipe out surplus liquid overflowing from the cell.
2. Introduce the cell in the heavy base socket and fasten it with the assistance of a screw provided on its side.
3. Attach the high frequency generator through cell by coaxial cable presented with the instrument. In ultrasonic interferometer frequency selector knob should be placed at needed frequency.
4. Move the micrometer gradually in any clockwise or anticlockwise direction till the anode current on the ammeter on the high frequency generator displays a maximum or minimum.
5. Note down the reading of micrometer equivalent to the maximum or minimum in microammeter.
6. Continue to increase the micrometer setting, noting the reading at each maximum. Count any number of maxima and call it as n. Subtract the reading at the first maximum from the reading at the last maximum. This will make the measurement accurate and we can say, $d = D/(n–1)$.

   Note down this value as,

$$D = \frac{(n-1)\lambda}{2}$$

Then calculate the velocity of wave through the medium as,

$$v = \lambda f = \frac{2Df}{(n-1)}$$

NOTES

7. Knowing the density of the medium, the adiabatic compressibility can be calculated using the equation,

$$\beta = \frac{1}{\rho v^2}$$

Observations

Least count of the micrometer: ……..mm

Frequency of the ultrasound used (*f*): …….Hz

n = ... , *D* =.....mm.

v = ... ms-1.

Observation Table

S.No	Micrometer Reading (mm)	Anode Current (μA)

Precautions

1. Do not switch on the generator without filling the experimental liquid in the cell.
2. Remove experimental liquid out of cell after use. Keep it cleaned and dried.
3. Keep micrometer open at 25mm after use.
4. Avoid sudden rise or fall in temperature of circulated liquid to prevent thermal shock to the quartz crystal.

5. While cleaning the cell, care should be taken not to spoil or scratch the gold plating on the quartz crystal.
6. Give your generator 15 seconds warming up time before the observation

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13. BABINET COMPENSATOR

Introduction

Double refraction, also called birefringence is an optical property in which a single ray of unpolarized light entering an anisotropic medium is split into two rays, each traveling in a different direction. One ray (called the extraordinary ray) is bent, or refracted, at an angle as it travels through the medium; while the other ray (called the ordinary ray) passes through the medium unchanged. This property can be measured using a Babinet compensator continuously variable zero-order retarder (wave plate) that can be used over a broad spectral range.

Theory

In case of double refraction, the ordinary ray and the extraordinary ray are polarized in planes vibrating at right angles to each other. Additionally, the refractive index (a number that determines the angle of bending specific for each medium) of the ordinary ray is observed to be constant in all directions; on the other hand, the refractive index of the extraordinary ray varies according to the direction taken because it has components that are both parallel and perpendicular to the crystal's optic axis. Because the speed of light waves in a medium is equal to their speed in a vacuum divided by the index of refraction for that particular wavelength, an extraordinary ray can move faster or slower than an ordinary ray.

Electromagnetic radiation propagates through space with oscillating electric and magnetic field vectors alternating in sinusoidal patterns which are perpendicular to one another and to the direction of wave propagation. As visible light is composed of both electrical and magnetic components, the velocity of light through a substance is significantly determined by the electrical conductivity of the material. Light waves travelling through a transparent crystal must interact with localized electrical fields during their journey. The relative speed at which electrical signals travel through a material varies with the type of signal and its interaction with the electronic structure, and is calculated by a property defined as the dielectric constant of the material. The relationship defining the interaction between a light wave and a crystal through which it passes is governed by the inherent orientation of lattice electrical vectors and the direction of the wave's electric vector

component. Therefore, a meticulous consideration of the electrical properties of an anisotropic material is fundamental to the understanding of light wave interaction with the material as it propagates through.

NOTES

Optical Path Difference

The optical path difference is a classical optical concept related to birefringence, and is defined by the relative phase shift between the ordinary and extraordinary rays as they emerge from an anisotropic material. In general, the optical path difference is calculated by multiplying the material thickness by the refractive index, but considering the medium is homogeneous and does not contain significant refractive index deviations or gradients. This quantity and birefringence, is usually expressed in nanometers and grows larger with increasing specimen thickness. For a material with two refractive index values (n(1)and n(2)), the optical path difference (D) is determined from the equation:

$$\text{Optical Path Difference } D = (n_1 - n_2) \bullet t \text{ (Thickness)}$$

For considering the phase relationship and velocity difference between the ordinary and extraordinary rays after they pass through a birefringent crystal, a quantity referred to as the relative retardation is often determined. As described above, the two light rays are oriented so that they are vibrating at right angles to each other. Each ray will experience a slightly different electrical environment (refractive index) as it enters the crystal and this will affect the velocity at which the ray passes through the crystal. Due to difference in refractive indices, one ray will pass through the crystal at a slower rate than the other ray. In other words, the velocity of the slower ray will be retarded compared to the faster ray. This retardation value can be quantitatively determined using the following equation:

$$\text{Retardation } (\Gamma) = \text{Thickness } (t) \times \text{Birefringence } (B)$$

Experimental Detail

A Babinet-Soleil Compensator is a continuously variable zero-order retarder (wave plate) that can be used over a broad spectral range. The variable retardance is attained by adjusting the position of a long birefringent wedge with respect to a short fixed birefringent wedge. The wedge angle and fast axis orientation is the same for both wedges so as to hve uniform retardance across the entire clear aperture of the Babinet compensator.

A compensator plate is connected to the fixed wedge, with its fast axis orthogonal to both the fast axis of the wedges and the propagation direction of the light. When the long birefringent wedge is arranged such that the total thickness of the two stacked wedges is equal to the thickness of the

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compensator plate, the net retardance of light passing through the Soleil-Babinet compensator is zero. The position of the long wedge can then be adjusted with a micrometer in order to create a retardance transmitted beam of light.

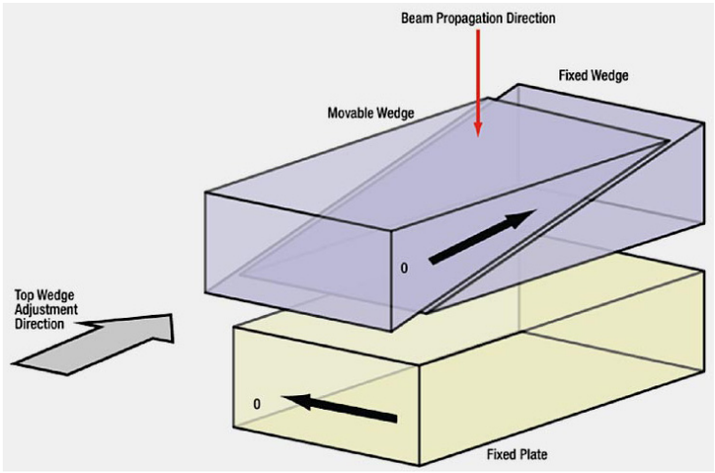


Fig. 1: *Experimental Setup for the Babinet Compensator*

Measurement of the Sample Birefringence

In 'Babinet Compensator' two wedges shaped Quartz crystals cut along its two different axes as shown in the Figure 1.

On such a crystal monochromatic plane polarized light is allowed to fall. The plane polarized light gets refracted and the O-rays and E-rays that are produced interfere with each other to form fringes. These fringes can be observed.

- The birefringent material is placed after the polarizer on which first the plane polarized light is allowed to fall.
- The O-rays and E-rays coming out of the material is allowed to fall on Quartz crystal of the Babinet compensator. Inside the compensator quartz crystal these rays further refract and hence the original fringes get shifted.
- By measuring the increase in fringe shift, birefringence of the material placed between the polarizer and the compensator can be estimated.

Analysis

Velocity of light in a medium is defined as,

$$V_{\text{medium}} = c/n$$

Where 'c' is velocity of light in vacuum 'n' is refractive index of the medium.

NOTES

Because of double refractive index the velocities of light in two different directions are different. Hence velocity along optical axis (X-axis) $V_{//} = c/n_0$

And similarly, $V_{//} = c/n_e$

And the path difference can be written as,

$$\Delta = (n_o - n_e)t$$

If this path difference is integral multiple of wavelength $\Delta = n\lambda$

The path difference due to second birefringent material is,

$$\Delta = (\lambda/\beta)\delta\beta$$

Where $\delta\beta$ is the fringe shift with second material, β is fringe width without the second material, t is the thickness of the second material and λ is wavelength of the light used.

Then the difference in refractive indices along two directions can be obtained as,

$$(n_o - n_e) = (\lambda/\beta)\delta\beta\, t$$

Experiment: To Determine the Birefringence of MICA using a Babinet Compensator.

Apparatus Required

- Polarizer
- Babinet-Soleil Compensator
- MICA Sheet
- Light Source (He – Ne LASER)
- Holder for Wave Plates
- Analyser

Procedure

- Switch on the LASER.
- Carefully mount the analyser and detector on the optical table.
- Setup the apparatus as shown in the Figure 1.
- Using the micrometer of The Babinet's compensator, the fringe width is measured.
- MICA sheet is placed between the polarizer and compensator, so there will be fringe shift.
- Measure the fringe shift through micrometer.
- Use different MICA sheets and try to match results.

NOTES

Precautions

- LASER should be handled carefully.
- A uniform thickness MICE sheet should be used in experiment.

14. TO DETERMINE THE HALF-LIFE OF A RADIOACTIVE ELEMENT.

Introduction

Geiger-Müller (GM) counters were invented by H. Geiger and E.W. Müller in 1928 and are used for the detection and measurement of all types of radiation: alpha (α), beta (β) and gamma (γ) radiation. it is extensively used in applications, such as radiation dosimetry, radiological protection, experimental physics, and the nuclear industry. All kinds of nuclear radiations, whether they are charged particles or gamma rays, will ionize atoms/molecules while passing through a gaseous medium. This ionizing property of a nuclear radiation is exploited for its detection.

Theory

The apparatus comprises of two parts, the Tube and the (Counter + Power Supply). The Geiger-Mueller tube is cylindrical in shape, with a wire down the center. The (counter + power supply) have voltage controls and timer options to accurately count number of particles (Refer Figure 1).

Working Principle

1. When ionizing radiation, such as an alpha, beta or gamma particle enters the tube, it can ionize, some of the gas molecules in the tube.
2. From these ionized atoms, an electron is knocked out of the atom, and the remaining atom is positively charged.
3. The high voltage in the tube produces an electric field inside the tube.
4. The electrons that were knocked out of the atom are attracted to the positive electrode, and the positively charged ions are attracted to the negative electrode.
5. The electrons now cause further ionization by virtue of the acceleration due to the intense electric field. These secondary ions can produce other ions and these in turn still other ions before reaching the electrodes. This cascading effect produces an avalanche of ions.
6. This produces a pulse of current in the wires connecting the electrodes, and this pulse is counted. Once a pulse is counted, the charged ions become neutralized, and the Geiger counter is ready to record another pulse.

7. In order for the Geiger counter tube to restore itself quickly to its original state after radiation has entered, a gas is added to the tube.
8. For proper use of the Geiger counter, one must have the appropriate voltage across the electrodes. If the voltage is too low, the electric field in the tube is too frail to cause a current pulse. If the voltage is very high, the tube will undergo continuous discharge, and the tube can be damaged. Usually the manufacturing company recommends the correct voltage to use for the tube.

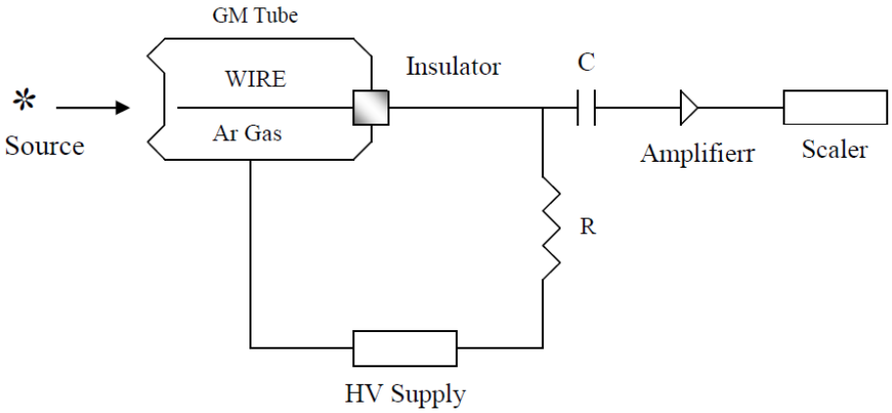


Fig. 1: *Schematic Diagram of the G-M Tube and the Associated Electronics*

Efficiency of the Geiger-Counter

The efficiency of a detector is given by the ratio of the (Number of particles of radiation detected)/(Number of particles of radiation emitted): $\varepsilon \equiv$ Number of particles of radiation detected number of particles of radiation emitted. This definition for the efficiency of a detector is also used for our other detectors. Efficiency of Geiger counter system is usually very small, because a gas is used to absorb the energy. A gas is not very dense, so most of the radiation passes right through the tube without ionizing. Unless alpha particles are very energetic, they will be absorbed in the cylinder that encloses the gas and will never be able to make it into the G-M tube. If beta particles enter the tube they have the most probable chance to cause ionization. Gamma particles themselves have a very low chance of ionizing the gas in the tube. Gamma particles are detected only when they scatter an electron in the metal cylinder around the gas into the tube. So although the Geiger counter can detect all three types of radiations, it is most efficient for beta particles and not very efficient for gamma particles.

Statistics of Radioactive Decay Process

Radioactive decay is a random process. Consequently, any measurement related to recording the radiation emitted in a nuclear decay is subject to some degree of statistical fluctuations. Although each measurement (number

of decays in a given interval) for a radioactive sample is independent of all previous measurements, for a large number of individual measurements the deviation of the individual count rates from the average count rate behaves in a known manner. Small deviations from the average are much more likely than large deviations. These statistical fluctuations in the nuclear decay are understood from the statistical models based on Poisson distribution or Gaussian (Normal) distribution. If we observe a given radioactive nucleus for a time t and define the success as "the nucleus decays during the process" then the probability of success "p" is given by $(1- e^{-\lambda t})$.

The Poisson distribution is applicable when the success probability p is small and the number of successes (i.e., number of counts measured) is also small (say <30). When the average number of successes becomes comparatively large (say > 30) we can use the Gaussian model of distribution. Since in most of the experimental cases the count rates are reasonably large (few tens of counts per second) the Gaussian model has become widely applicable to many problems in counting statistics.

The Poisson Distribution

As explained above it is applicable when p <<1 and the number of successes are very few.

$$P(y) = \frac{(\bar{y})^y e^{-\bar{y}}}{y\,!}$$

In this case the standard deviation is given by,

$$\sigma_p = \sqrt{\bar{y}}$$

Half-Life of a Radioactive Material

The decay of radioactive atoms occurs at a uniform rate. There is no way to slow it down. The half-life of a radioactive element is defined as the time needed for half of the material to decay.

The change in the number of radioactive atoms is a very systematic process. If we know the number of atoms present and their decay constant (probability of decay per unit time), then we can calculate how many atoms will remain at any future time. This can be written as the equation

$$N(t) = N - \lambda N \Delta t\,, \qquad \ldots(1)$$

where $N(t)$ is the number of atoms that will be present at some time t, N is the number of atoms present at current time, λ is the decay constant, and Δt is the elapsed time.

But $N(t)$-N is the change in the number of radioactive isotopes of the original type present, so we can define,

NOTES

$$\Delta N = N(t) - N = -\lambda N \Delta t \quad ...(2)$$

Dividing both sides of the equation gives,

$$\frac{\Delta N}{\Delta t} = -\lambda N \quad ...(3)$$

Or

$$\frac{dN}{dt} = -\lambda N. \quad ...(4)$$

The solution to this equation is,

$$\ln(N) - \ln(N_0) = -\lambda t \quad ...(5)$$

Finally, we can solve for the half-time

$$t_{1/2} = \frac{ln(2)}{\lambda} \quad ...(6)$$

Experiment: To calculate the Statistical Probability, Absorption measurements, Half-life using a G-M Counter.

Apparatus Required

1. Geiger-Müller (GM) Tube and Stand
2. Radioactive Source
3. Shelf Stand, Serial Cable, and a Source Holder

Procedure

1. Set the operating voltage of the Geiger counter at its appropriate value.
2. Do not put any source in the lead castle. Also remove all the sources in the near vicinity of the castle.
3. First do a run without a radioactive source to calculate your background level.
4. Place one of the g sources (137Cs or 60Co) far enough away from the window of the Giger tube so that approximately 3000 counts are recorded in a time period of 30 s. Take 200 independent readings of the counts for a preset time of 60 s.
5. Record the data to a file on disk or into a data table.
6. You may wish to do a second trial if time allows.
7. Determine frequency of occurrence $n(y)$ which is the number of measurements in which y = 10, 20,30 , 50, 100 ….counts have been observed and plot the experimental distribution $n(y)$ versus y to see the kind of Poisson distribution.

NOTES

Analysis

The variable λ is the decay coefficient. If you have plotted Equation (1), then the slope from the linear regression is the negative of λ,

$$\lambda = -(slope)$$

From Equation (6), you can calculate the half-life:

$$t_{1/2} = \frac{ln(2)}{\lambda}$$

Do error analysis using proper error propagation.

Precautions

- Hazardous voltages can exist at the GM and SCINT connectors. Make sure that the high voltage is set to zero or that the instrument is OFF before connecting or disconnecting a detector.
- While performing an experiment with one radioactive sample other sources should not be present nearby. They should be put behind the lead shield.
- Hold the radioactive sources with care. Do not touch the centre of samples with bare hands.
- While dealing with liquid radioactive samples please use hand gloves.
- Do not put your mobile phone near the detector. It may add some counts to the signal.

15. ELLIPTICAL FRINGES

Introduction

In an experiment, Marie Alfred Cornu showed that the interference phenomenon in optics could be used to measure the deformation of a solid under a load. It was very much interesting to know about Young's modulus and Poisson's ratio for a transparent material Young's modulus and Poisson's ratio for a transparent material by counting the interference fringes.

Theory

When a plano-convex lens rests on a uniformly bent bar of glass, an air film is formed between the two surfaces. On illuminating the air film with monochromatic light, a system of elliptical fringes (longitudinal and transverse) around the point of contact of the glass bar is obtained.

It is an experimental observation that *f* for a large numbers of materials, for sufficiently small extensions the force is proportional to the extension.

$$F \alpha \Delta L \quad ...(1)$$

Hereby we give a linear relationship between the force and the extension. Due to the virtue of this linear relation the principle of superposition is obeyed by the internal forces. This empirical relation is known as Hooke's law. For the whole of our experiment, we assume that Hooke's law is being obeyed and that we are within the elastic limits of the material. The Young's modulus, one of the elastic constants, is defined as the ratio of stress to strain.

$$Y = \frac{\frac{F}{A}}{\frac{\Delta l}{l}}$$

- A $\Rightarrow$ Area
- 1 $\Rightarrow$ Length of the non-extended rectangular block

Thus, for a rectangular block, Young's modulus has the form,

$$Y = \frac{Fl}{A\Delta l} \qquad ...(2)$$

Consider a two-dimensional rubber material; if you stretch it, it gets in that direction of the force being applied. As the stretching does not change the net area of the rubber material, there must be a contraction to be observed somewhere in the strip of rubber. There is another part to Hooke's law: When you stretch a block of material in one direction it contracts at right angles to the stretch. This phenomenon cannot be explained by Equation (1). Because this equation predicts only that the force in one direction produces an effect only about that direction. To explain the contraction of rubber in a perpendicular direction to that of the force, we would have to consider expressing elasticity as a tensorial property. Here the force provided on the material can be seen to have effects in other directions too.

$$\frac{\Delta w}{w} = \frac{\Delta h}{h} = -\sigma\frac{\Delta l}{l} \qquad ...(3)$$

w is the width and h is the height of the rectangular block. σ is another elastic constant called the Poisson's ratio. Its range should be in $-1 < \sigma <$ 0:5 so that the shear and the Bulk modulus of elasticity stay positive. These two elastic constants are sufficient for describing the elastic properties of a homogeneous and isotropic material. For the other cases, we need to make use of tensors.

Cornu's Method: The apparatus shown in Figure 1 has a glass beam bent under loads at its ends and balancing on the two knife edges. A glass plate is placed on the center of the glass beam resulting in the making of an air wedge enclosed between these two surfaces. An interference fringe pattern is produced due to the interference of the light rays getting reacted from the bottom of the glass plate with the light rays reacted from the top of the

glass slab. We know that on stretching a piece of rubber, we can observe that the width of the rubber gets narrowed near the center of the strip which is quantized by the Poisson's ratio. In analogy to this, in two dimensions, the bending of the glass slab in the direction of the weight gives rise to a transverse bending of the glass beam as a cup, opposite to the bending of the glass slab visibly seen. This gives a saddle like structure (not visible through naked eyes in this experiment) to the glass beam.

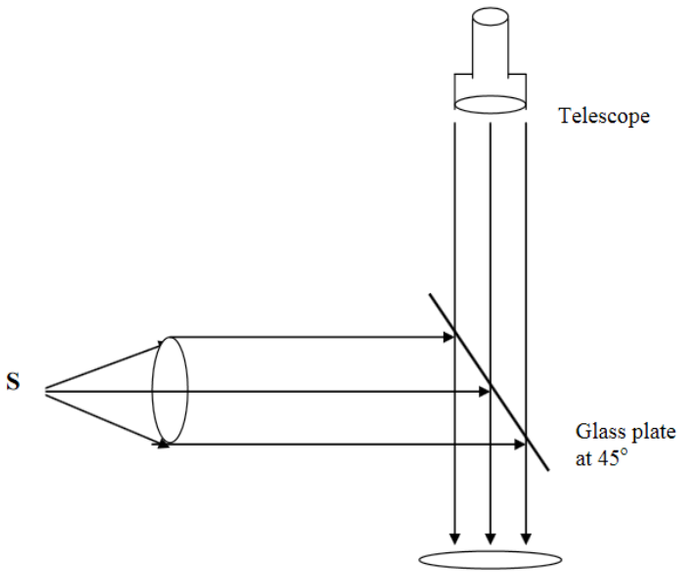


Fig. 1: *Cornu's Method*

The center of this sphere (if the two-dimensional surface is completed) will be on the positive Z-axis while the center of the sphere visibly seen will be in the negative Z-axis. If we take x and y to be the longitudinal and transverse direction respectively, then let us name the corresponding radii of curvature as R_x and R_y, respectively.

Let R_1 be the longitudinal radius of curvature of the beam. The internal bending moment caused by extension of the surface above the bar and compression below the bar is given by $\frac{YAK^2}{R_1}$. where, Y is the Young's modulus, $A = ab$, is the cross-sectional area of the bar, $K = \frac{b}{\sqrt{12}}$, the radius of gyration for the rectangular cross section. In equilibrium condition, the internal bending moment must be balanced by the moment due to weight $m_1 g$ attached to its ends (Refer Figure 2).

$$m_1 g = \frac{YAK^2}{R_1} \qquad ...(4)$$

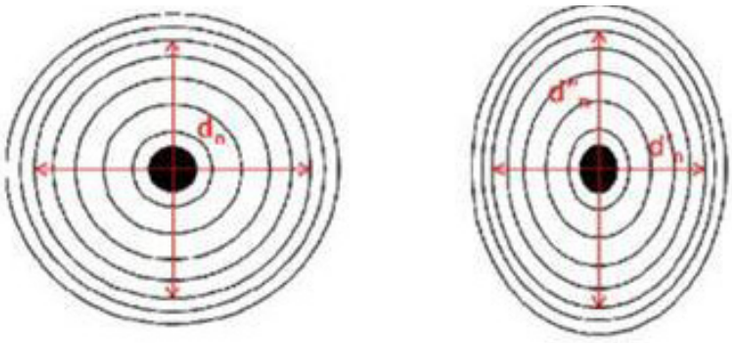
NOTES

On rearranging, we get, Young's modulus,

$$Y = \frac{12 m_1 g l R_1}{a b^3} \quad ...(5)$$

Also when the bar undergoes longitudinal bending, it also undergoes a lateral bending, resulting in lateral strain R_2. The ratio between these two quantities is the Poisson's ratio and is given by,

$$\sigma = \frac{R_1}{R_2} \quad ...(6)$$



$W = 0$ $W = m_1 g$

Fig. 2: *Cross-Sectional Area of the Bar*

The longitudinal bending R_1 can be found out using the equation,

$$R_1 = \frac{1}{4n\lambda} \frac{d_n'^2 \, d_n^2}{(d_n^2 - d_n'^2)} \quad ...(7)$$

where d_n' and d_n are the diameters of the nth ring with mass and without mass in the longitudinal direction. Similarly,

$$R_2 = \frac{1}{4n\lambda} \frac{d''^2_n \, d_n^2}{(d_n^2 - d''^2_n)} \quad ...(8)$$

where $d_n'^2$ and d_n are the diameters of the nth ring with mass and without mass in the transverse direction. So from the values of the diameter of rings with mass and without mass, we calculate R_1 and R_2. From those values of R_1 and R_2, we calculate Young's modulus $Y = \frac{12 m_1 g l R_1}{a b^3}$ Poisson's ratio, $\sigma = \frac{R_2}{R_1}$ and Bulk modulus, $b = \frac{Y}{3(1-2\sigma)}$.

Experiment: To determine Young's modulus and Poisson's ratio of a glass slab using Cornu's method.

Apparatus Required: Optically plane glass plate**,** Travelling Microscope, Sodium lamp, Glass beam, Plano-Convex lens**,** Slide caliper and screw gauge, Pair of knife edges, Hangers, Loads, etc.

NOTES

Procedure

1. The width, length, and depth of the glass beam are measured using vernier calipers, screw gauge, and a measuring scale respectively. The center of the glass beam and the slide placed on it is marked.
2. The glass beam is placed on the two knife edges symmetrically and the distance between the knife edge and the point of suspension (considering the middle point of the slid of the hanger).
3. The hanger is loaded to weigh 250g.
4. The glass plate is placed on the beam such that the center of the glass plate coincides with the center of the glass beam.
5. The diffraction pattern can be observed from naked eyes and the microscope is brought to that position and focussed on the diffraction pattern produced. The hyperbolic fringes must be seen to be symmetrical about the *X* and the *Y* axis of the eyepiece.
6. Readings are taken of the position of each dark fringe. For X-axis, the readings are taken for the dark fringes on both the sides of the origin. Similar readings are taken for the Y-axis too seeing that the eyepiece wire is tangential to the fringes.
7. The experiment is repeated now for the weight 300g.
8. The experiment is repeated for both the weights by placing the Plano-convex lens (with the convex lens on the bottom) and similar readings are taken.

Observations

To Find the Thickness of Perspex Beam using Screw Gauge

Zero correction =

No	MSR	VSR	Total Reading (cm)

Thickness of Perspex beam, b = ... mm

To Find the Breadth of Perspex Beam using Vernier Calipers

No	MSR (cm)	VSR	Total Reading (cm)

Breadth of plate, a = ... cm

To Find the Diameter of Rings in Horizontal Direction

λ = ...nm, l = ... cm

Order,n	Mass(g)	Microscope Reading		Diametre, d_n (cm)	d_n^2	$d_n^2 - d_n''^2$	$d_n^2\ d_n''^2$
		Left	Right				
	0						
Order,n	Mass(g)	Left	Right	Diametre, d_n' (cm)	$d_n'^2$	$d_n^2 - d_n'^2$	$d_n^2\ d_n'^2$
	100						

Longitudinal bending $R_1 = \frac{1}{4n\lambda}\frac{d'^2_n\ d^2_n}{(d^2_n - d'^2_n)}$

To Find the Diameter of Rings in Vertical Direction

Order,n	Mass(g)	Microscope Reading		Diametre, d_n (cm)	d_n^2	$d_n^2 - d_n'^2$	$d_n^2\ d_n''^2$
		Up	Down				
	0						
Order,n	Mass(g)	Up	Down	Diametre, d_n'' (cm)	$d_n''^2$	$d_n^2 - d_n''^2$	$d_n^2\ d_n''^2$
	100						

Longitudinal bending $R_2 = \frac{1}{4n\lambda}\frac{d''^2_n\ d^2_n}{(d^2_n - d''^2_n)}$

Results

For a given plate:

1. Young's Modulus, Y = ...Nm^{-2}
2. Poisson's Ratio, σ = ...
3. Bulk Modulus, b = ...Nm^{-2}

Precaution

1. The glass plate must be at 45^{o} of the horizontally incident light.
2. Count the fringes carefully.
3. Make sure that load > 400 grams is not exerted on the glass beam.